Neurmorphic Architectures

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Historical Highlights

Analog VLSI

- Carver Mead and his students pioneered the development aVLSI technology for use in neural circuits
- They developed a silicon retina which electronically emulated the first 3 layers of the retina

Image from [3]

Artificial Neural Network Chips

- Early neuromorphic architectures were artificial neural network chips
- Examples:
  - ETANN : (1989) Entirely analog chip that was designed for feed forward artificial neural network operation.
  - Ni1000 : (1996) Significantly more powerful than ETANN, however has narrower functionality

SYNAPSE-1 System Architecture

SYNAPSE-1 is a modular system arranged as a 2D array of MA16s, weight memories, data units, and a control unit

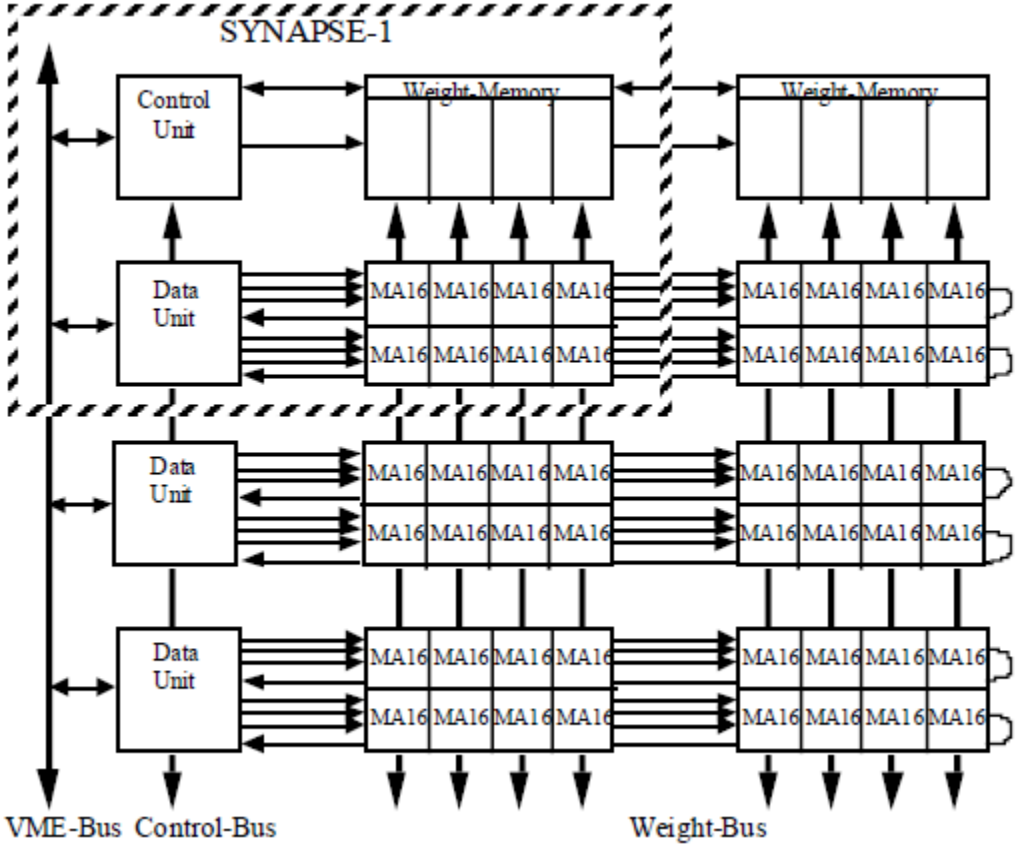


Image from [6]

Modern Architectures: Custom Circuits

Neurogrid

- (2005) Neurogrid is a multi-chip system developed by Kwabena Boahen and his group at Stanford University [9]
  - Objective is to emulate neurons
  - Composed of a 4x4 array of Neurocores
  - Each Neurocore contains a 256x256 array of neuron circuits with up to 6,000 synapse connections

The FACETS Project

- (2005) Fast Analog Computing with Emergent Transient States (FACETS)
  - A project designed by an international collective of scientists and engineers funded by the European Union
  - Recently developed a chip containing 200,000 neuron circuits connected by 50 million synapses.

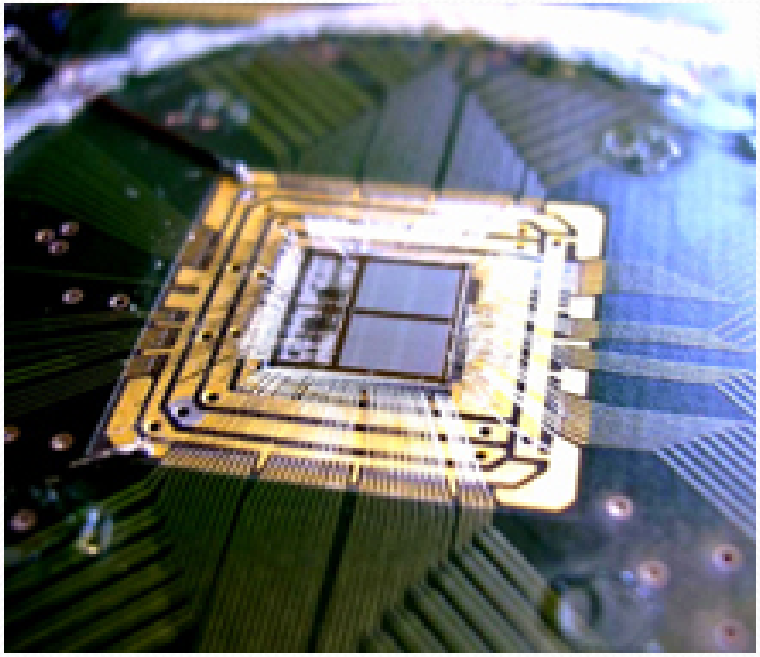


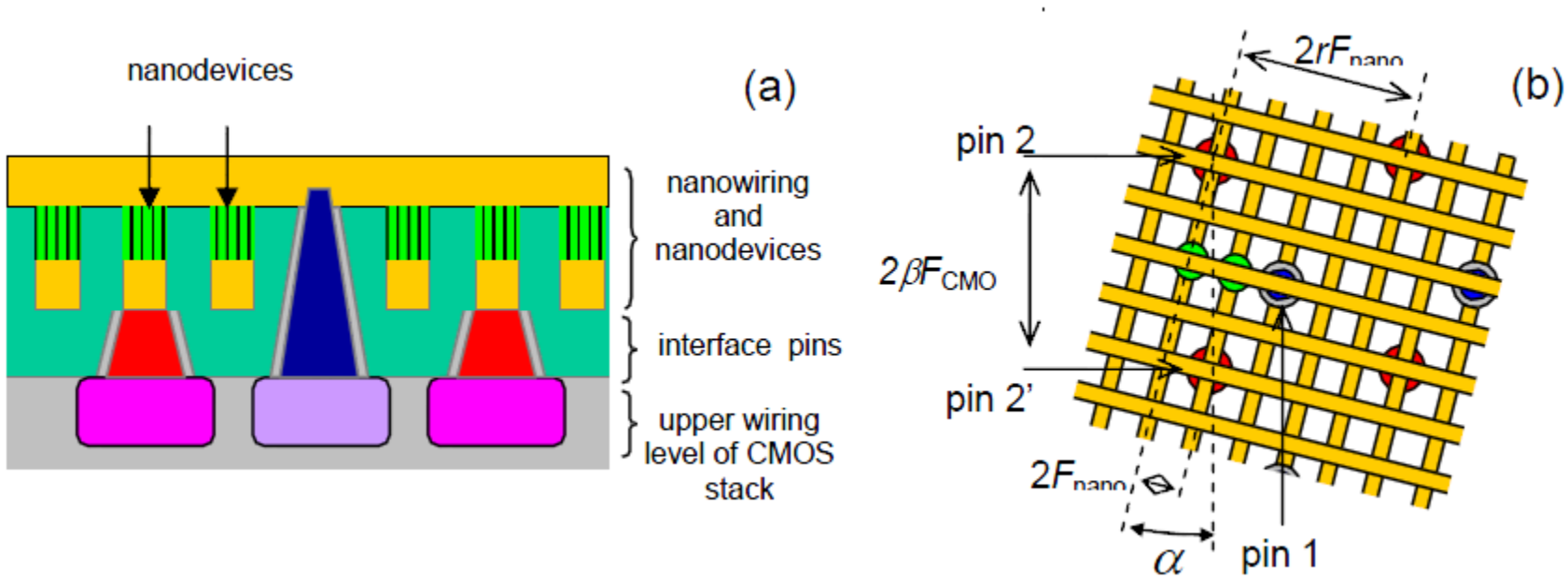
Image from [9]

Torres-Huitzil: FPGA Model

- Torres-Huitzil et. al (2005) designed an hardware architecture for a bio-inspired neural model for motion estimation.
  - Architecture has 3 basic components which perform spatial, temporal, and excitatory-inhibitory connectionist processing.
  - Observed approximately 100 x speedup over Pentium 4 processor implementation for 128x128 images

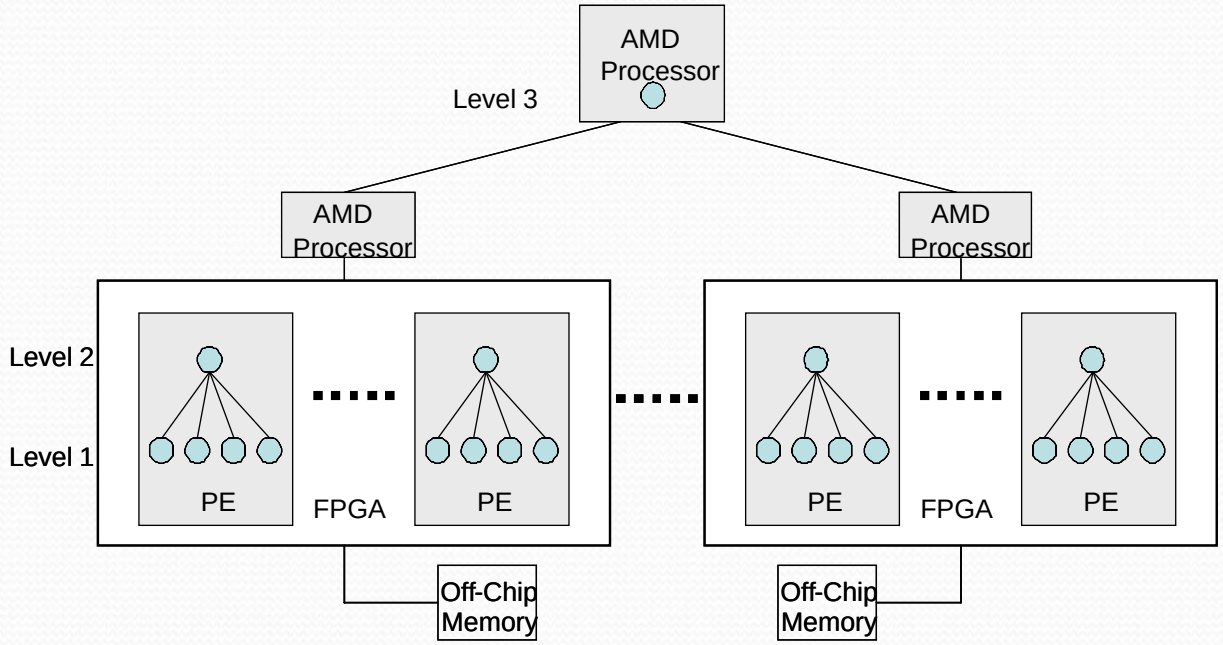
CMOL based design

- Developed by Dan Hammerstrom

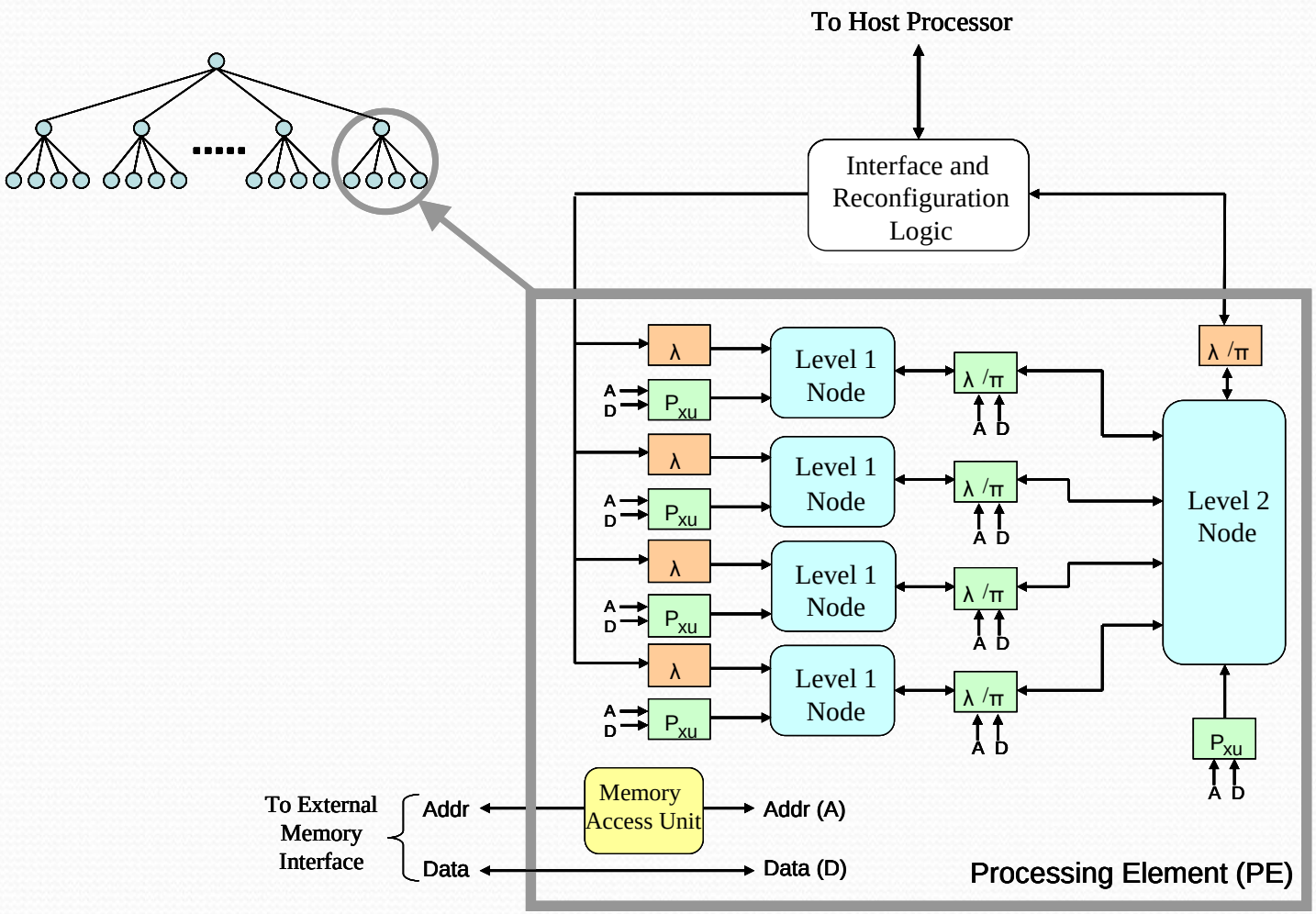


HTM on FPGAs

- Implemented on a Cray XD1



PEs on FPGA


To Host Processor
Interface and Reconfiguration Logic
λ
A
D
Pxu
Level 1 Node
λ /π
Level 2 Node
Memory Access Unit
To External Memory Interface
Addr
Data
Addr (A)
Data (D)
Processing Element (PE)

Large Scale Simulations

- IBM:
  - Blue Brain Project: IBM & EPFL (Switzerland)
  - IBM Almaden Research Center
- Los Alamos National Lab
- Air Force Research Laboratory (Rome, NY)
- Academia:
  - Portland State University
  - Royal Institute of Technology (KTM, Sweden)

AFRL PS3 Cluster

For more information

- Visit Institute of Neuromorphic Engineering:
  - http://www.ine-web.org/

References

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[12] C. Torres-Huitzil, et. al. "On-chip Visual Perception of Motion: A Bio-inspired Connectionist Model on FPGA, " Neural Networks Journal, 18(5-6):557-565, 2005.