Syllabus
CPSC321 Computer Architecture
Fall 2004

Instructor	Dr. Andreas Klappenecker
Office	HRBB 509B
Office hours	TW 10:15pm-11:15pm or by appointment
Course homepage	http://faculty.cs.tamu.edu/klappi/arch/arch.html

Learning Objectives. At the end of this course you should

- know the early historical developments of computers;
- be able to understand basic hardware and software components;
- have a working knowledge of the MIPS assembly language;
- have developed programming skills in MIPS assembly language;
- know the basics of functional architecture design of computers;
- know the rudiments of the hardware description language Verilog;
- be able to model the behavior of architectural components in Verilog;
- be knowledgeable about the design of I/O modules, control unit, and arithmetic logic unit;

Prerequisites. Basic computer and programming skills, including fluency in at least one high-level programming language; basic knowledge of digital logic design, ELEN 248 or ELEN 220.

Course materials. The **required textbook** for this course is

> D. Patterson, J. Hennessy: *Computer Organization and Design: The Hardware-Software Interface*, Morgan Kaufman Publishers, 2nd edition, 1997 (a newer edition is now also available, but we still use the old one).

I recommend the book by Robert Britton on *MIPS Assembly Language Programming*, Prentice Hall, 2003, if you prefer a more detailed exposition of the MIPS assembly language, and the book by S. Brown and Z. Vranesic on *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill, 2003, if you want to refresh your memory on digital logic design. Numerous other references will be mentioned during the course.

Grading. The course has two exams, but no final exam. An integral part of the course are lab assignments, possibly quizzes, various assembly language and hardware description language projects. The grade will be calculated as follows:

> **Exams** (25% each) 50%, **Projects** 30%, **Assignments and Quizzes** 20%

The dates of all major examinations will be announced in class. The course grades will be assigned according to the scale **A** for 90%-100% of total points, **B** for 80%–89%, **C** for 70–79%, **D** for 60%–69%, and **F** otherwise. A curve might be applied if the class average deviates significantly from the expected value.

Attendance Policy. Lecture and labs attendance is strongly enouraged. Unavoidable absences are understood, but each student is responsible for missed material. For excused absences, an opportunity will be provided to make up any graded work that was missed. For unexcused absences, a grade of zero will be assigned for a missed assignment or exam. Missed exams will be rescheduled without penalty for an excused absence. If you are going to be absent when a lab is due you should try to turn in the lab early. If that is not possible, be sure to request an extended lab turn-in time from your Teaching Assistant.

To request approval of an absence, send me an e-mail explaining the reason for the absence. Tell me if you believe it is a university excused absence. I will approve most requests provided I receive them **prior** to the class or lab. If advance notification is not possible (e.g. unexpected illness) send the e-mail within 48 hours of the absence and be sure to explain why you were not able to notify me in advance. For illness, follow-up the e-mail by submitting a note from a doctor or clinic to my office.

Lab Assignments. Submit your lab assignments as instructed by your Teaching Assistant.

Scholastic Dishonesty. Scholastic dishonesty will not be tolerated. Examinations are meant to measure the knowledge or skill of each individual, so giving or receiving unauthorized assistance during tests and quizzes is cheating. It is assumed that college students know what is honest and what is not. Any identified instances of scholastic dishonesty will be dealt with in accordance with the procedures outlined in the University Student Rules.

Students with Disabilities. The Americans with Disabilities Act is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact the Department of Student Life, Services for Students with disabilities in room 126, Koldus, or call 845-1637

Course Contents. A tentative list of topics covered in this class includes:

• Introduction; history; the five components of a computer; performance; technology and delay modeling	Chapter 1, 2 (partially)
• Introduction to Instruction Set Architecture (ISA) Design; MIPS ISA; translation of high-level language constructs into MIPS; Assemblers, object code generation, linking and executable loading; run-time execution Environment	Chapter 3, Appendix A.
• Review of digital-logic design for combinational circuits	Appendix B.
• Introduction to hardware description languages (Verilog) and the design–simulation process; overview of computer arithmetic and ALU design; structural designs in Verilog	Chapter 4
• Review of digital-logic design for sequential circuits; register-transfer level description of systems	Appendix B.
• Single-cycle datapath and control; multi-cycle datapath and control; micro-programming and hard-wired control units; behavioral HDL description of systems; exceptions handling	Chapter 5, Appendix C
• Intro to pipelining; pipelined MIPS datapath; pipeline hazards: structural, control, data; hazard detection and resolution; pipelining control; exceptions handling	Chapter 6

Time permitting, we might also cover

• Overview of SRAM and DRAM design; memory hierarchy; cache memory design	Chapter 7
• Virtual memory	Chapter 7
• Buses, I/O sub-systems and devices	Chapter 8
• Future architectures: Quantum computers	

Please consult the class homepage for reading assignments!