

CURRICULUM VITAE

Personal Information

Name: Rabi N. Mahapatra

Current Title: Associate Professor

Address: Department of Computer Science
Texas A&M University
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Education

Ph.D., Computer Engineering, *Indian Institute of Technology*, Kharagpur, 1992.

Dissertation: *Performance Analysis of Multiprocessor Architectures for some Orthogonal Transforms.*

M.S., Electronics Systems, Electrical Engineering, *Sambalpur University*, India 1984.

Thesis: *A Microprocessor-based Rectangular Transforms.*

B.Sc Engg. (Hons), Electronics & Telecommunication Engg, *Sambalpur University*

Principal Areas of Interest

- **Embedded Systems:** Energy Efficient Design, Hardware-Software Codesign, and Real-Time systems.
- **System-on-Chip:** Network-On-Chip, Communication Synthesis for low-power and reliability.
- **VLSI Architecture:** Impact of Process Variation, Reconfigurable architectures and Application Specific Architectures.
- **Networking and Cyber Physical Systems:** IP Lookup Architecture, Sensor Network, Semantic Routing, and Middleware.

Professional Experience

Associate Professor: Department of Computer Science, *Texas A&M University*. (September 2001– present), Research focus involves problems related to Embedded Systems, Architecture and VLSI Design, Teaching Graduate & Undergraduates in computer science and engineering.

Academic Visitor: *IBM T.J Watson Research Center* (ARL, Austin). (June – August 2001), Design of Event Driven Power Model for PowerPC Architecture

Visiting Assistant Professor/Senior Lecturer/Research Associate Professor: Department of Computer Science, *Texas A&M University*, (September 1995–August 2001), Non-tenure-track teaching appointments.

Assistant Professor: Computer Engineering Group, Department of Electronics & Electrical Communication Engineering, *Indian Institute of Technology*, Kharagpur, India (April 1992– August 1995). Research and Teaching in Parallel & Distributed Processing.

Research Support

Contracts, Grants & Gifts

- 1) *A Comprehensive Methodology for Early Power-Performance Estimation of Nano-CMOS Digital Systems*. (September 2007 – August 2010)
Sponsor: CCF, National Science Foundation (NSF)
Involvement: Co- Principal Investigator
- 2) *Design of Robust and Energy Efficient Cyber-Physical Systems Using Dynamical Systems and Control Theory*. (September 2007 – August 2009)
Sponsor: CSR-CPS, National Science Foundation (NSF)
Involvement: Co- Principal Investigator
- 3) *Safety Analysis Framework of Microprocessors and SoCs in Avionics*. (August 2007 – July 2009).
Sponsors: FAA and AVSI (BAE, Boeing, GE Aviation, Honeywell, Lockheed Martin, Hamilton Sundstrand),
Involvement: Principal Investigator
- 4) *Power-aware Resource Management in Densely Packaged Distributed Real-Time Embedded Systems*. (September 2005 – August 2008)
Sponsor: National Science Foundation (NSF)
Involvement: Principal Investigator
- 5) *Microprocessors Evaluation for Avionics*, (August 2004- July 2006)
Sponsor: Department of Transportation (DoT), (FAA and AVSI)
Involvement: Principal Investigator
- 6) *Geostationary Imaging Fourier Transform Spectrometer (GIFTS) Star Tracker System*, (July 2002 – June 2003)

Sponsor: NASA - Langley Research Center

Involvement: PI, (Co- PI: M. Jacox from Commercial Space Center),

- 7) *Research on Embedded Systems,*” (September 2004 – May 2005),
Sponsor: Champion Innovation Inc.,
Involvement: Principal Investigator
- 8) *Codesign Research & Design in Computer Science Curriculum,* (2001 – 2003)
Sponsor: Ford Motor Company
Involvement: Principal Investigator
- 9) *Architecture Evaluation using Commercial Workload,* (January 2000 – December 2001)
Sponsor: Texas Advance Technology Program
Involvement: Senior Investigator, (PI: Laxmi Bhuyan)
- 10) *Embedded System Research & Development,* (2000-2001)
Sponsor: IBM Corporation
Involvement: Principal Investigator

Infrastructure Grants (External)

1. *Reconfigurable System Laboratory Design & Research,* (2002-2003)
Sponsor: Xilinx Corporation
Involvement: Principal Investigator, Gift Amount: \$244,295, (Devices and hardware)
2. *Academic Partnership Award,* (1999)
Sponsor: National Instruments
Involvement: PI, Award Amount: \$145,800, (Hardware and Software)
3. *Tools for Codesign Lab,* (2002)
Sponsor: MontaVista, Software & Tools of value \$25,000.00
4. *Senior Design Laboratory Building- Educational Equipment and Resources,* (1997-99)
Sponsor: Xilinx Corp., Involvement: PI, Amount: \$65,000.00 (Tools & Hardware)
5. *Microprocessor System Design Lab Developments,* PI: Mahapatra, Motorola Semiconductor Inc., Hardware/Firmware, \$20,000.00, Fall 1999.
6. *Senior Design Projects using WinCE Devices,* PI: Mahapatra, Microsoft Corp., Software and Devices, \$20,000.00, Fall 1999.

Publications (The * indicates the author to be a graduate student)

Book and Journal Editing

- [1] R. Mahapatra, Guest Editor, *Special Issue on “Embedded System Codesign”*, International Journal on Microelectronics, Elsevier Publication, November 2003.
- [2] R. Mahapatra, Editor, *“Trends in Information Technology,”* McGraw Hill Publications, 1998.

Peer Reviewed Journal

- [3] S. Acharya* and R. Mahapatra, "A Dynamic Slack Management Technique for Real-Time Distributed Embedded System," *IEEE Transactions on Computers*, to appear in 2007.
- [4] R. Singhal*, G. Choi and R. Mahapatra, "Data Handling Limits of On-Chip Interconnects," *IEEE Transactions on TVLSI*, Accepted for Publication.
- [5] S. Ahmad* and R. Mahapatra, "An Efficient Approach to On-chip Logic Minimization", *IEEE Transactions on VLSI*, to appear in 2007.
- [6] Mark Nolen* and R. Mahapatra, "A Time Division Multiplexed Test Delivery Methodology for Network-on-Chip Systems," *IEEE D&T*, Accepted for Publication.
- [7] D. Wu*, J. Hu and R. Mahapatra, "Antenna Avoidance in Layer Assignment", *IEEE Transactions on Computer Aided Design*, pp. 734-738, April 2006.
- [8] A. Rajaram*, J. Hu, W. Guo, R. Mahapatra and B. Lu, "Analytical Bound for Unwanted Clock Skew Due to Wire Width Variation," *IEEE Transactions on Computer Aided Design*, .25(9): 1869-1876 (2006).
- [9] A. Rajaram*, J. Hu, and R. Mahapatra, "Reducing Clock Skew Variability via Cross Links", to appear in *IEEE Transactions on Computer Aided Design*. 25(6): 1176-1182, June 2006
- [10] V. Kappagantula*, S. Acharya* and R. Mahapatra, "A Partitioning Algorithm for Power Constrained Reconfigurable Real-Time System," to appear in *Microprocessors and Microsystems Journal*, Elsevier Publication (Editor: Iain Bate).
- [11] R. Mahapatra and W. Zhao, "An Energy efficient Slack Distribution Technique for Multimode Distributed Real-time embedded Systems," *IEEE Transaction on Parallel and Distributed Systems* (TPDS), Volume 16, Issue 7, July 2005 pp.650 - 662.
- [12] V. C. Ravikumar*, R. Mahapatra and L. N Bhuyan, "EaseCAM: An Energy and Storage Efficient TCAM-based Router Architecture," *IEEE Transactions on Computer*, Vol.54, No.5, May 2005 pp.521-533.
- [13] A. Kumar* and R. Mahapatra, "An Integrated Scheduling and Buffer Management Scheme for Input Queued Switches with Finite Buffer Space," *Computer Communication Journal*, Elsevier Science Publication, Volume 29, Issue 1, pp. 42-51, December 2005.
- [14] V. C. Ravikumar*, and R. Mahapatra, "Ternary-CAM Architecture for IP Lookup Using Prefix Properties", *IEEE Micro*, April/May 2004, pp. 60-69.
- [15] S. Mahapatra* and R. Mahapatra, "Mapping of Neural Net Models onto Systolic Arrays", *Journal of Parallel and Distributed Computing*, Vol. 60, 2000, pp. 677-689.
- [16] S. Mahapatra*, R. Mahapatra and B. N. Chatterji "Mapping of Neural Network Models onto Massively Parallel Hierarchical Computer Systems," *Journal of System Architecture*, Elsevier Science Publisher, Vol. 45, No. 11, May 1999, pp. 919-929.

- [17] A. Pani*, G. P. Bhattacharjee and R. Mahapatra “Event Scheduling using Allen Algebra”, *Intl. Journal of Computer Mathematics (ICJM)*, Vol. 70,1998, pp. 87-97.
- [18] R. Mahapatra, A. Kumar* and B. N. Chatterji, “Performance Analysis of 2-D Inverse Fast Cosine Transform Employing Multiprocessors”, *IEEE Transaction on Signal Processing*, Vol.45, No.5, May'97, pp.1323 - 1335.
- [19] B. K. Das*, R. Mahapatra and B. N. Chatterji, “Modeling Hadamard Haar Transform Algorithm for Omega Connected Multiprocessor”, *Signal Processing*, Elsevier Science Publishers, Vol.58, No. 3, May 1997, pp. 293 - 301.
- [20] S. Mahapatra*, R. Mahapatra and B. N. Chatterji, “A Parallel formulation of Back Propagation learning on Distributed Memory Multiprocessors,” *Parallel Computing*, Elsevier Publishers, Vol., No.12, Feb. 1997, pp.1661-1675.
- [21] R. Mahapatra and S. Mahapatra*, “Mapping Neural Network Models onto Two-Dimensional Processor Arrays,” *Parallel Computing*, Elsevier Publishers, Vol. 22, No. 10, Jan. 1997, pp. 1345-1357.
- [22] C. R. Tripathy*, R. Mahapatra and R. B. Misra, “Reliability Analysis of Hypercube Multicomputers,” *Microelectronics and Reliability*, Elsevier Publishers, Vol.37 (6), 1997, pp. 885-891.
- [23] C. R. Tripathy*, S. Patra*, R. B. Misra and R. Mahapatra, “Reliability Evaluation of Multistage Interconnection Networks with Multistate Elements,” *Microelectronics and Reliability*, Elsevier Publishers, Vol. 36, No.3, 1996, pp. 423-428.
- [24] B. K. Das*, R. Mahapatra and B. N. Chatterji, “Performance Modeling of Discrete Cosine Transform for Star-Graph Connected Multiprocessors,” *Intl. Journal of Circuits Systems and Computers*, Vol. 6, No.6, 1996, pp. 635-648.
- [25] C.R. Tripathy*, R. Mahapatra and R. B. Misra, “Fuzzy Reliability Evaluation of Multistage Interconnection Network,” *Computer Science and Information*, Vol. 25, No. 4, Dec. 1995, pp.17-29.
- [26] R. Mahapatra and Sudipta Mahapatra*, “Modeling 2-D IFCT Algorithm on a Multistage Interconnection Network,” *Signal Processing*, Elsevier Publishers, Vol. 30, No.2, 1993, pp. 235-243.
- [27] R. Mahapatra and H. Pareek*, “Modeling a Fast Parallel Thinning Algorithm for Shared Memory SIMD Computers,” *Information Processing Letters*, Vol. 40, No. 5, Dec. 1991, pp. 257-261.
- [28] A. Dutta*, S.V. Joshi* and R. Mahapatra, “Modeling Morphological Thinning Algorithm for Shared Memory SIMD Computers,” *Parallel Processing Letters*, Vol.1, No.1, 1991, pp. 59-65.
- [29] R. Mahapatra, “Microprocessor Implementation of Fast Convolver,” *IETE Technical Review*, Vol.5, No.5, Aug. 1988, pp. 326-328.

Journal Articles (Revised or Under Review)

- [30] S. Mohanty, E. Kougianos and R. Mahapatra, "Hardware Assisted Solutions for Real-Time Watermarking," *Intl. Journal of Computers and Electronics*.
- [31] P. Bhojwani and R. Mahapatra, "Robust Concurrent On-line Testing of SoCs", *IEEE Transactions on VLSI*.
- [32] Y. Kim, R. Mahapatra, I. Park, and K. Choi, "Low Power Reconfiguration Technique for Coarse-Grained Reconfigurable Architecture," *IEEE Transaction on VLSI*.

Peer Reviewed Conference Publications

- [33] Yoonjin Kim* and Rabi N. Mahapatra, "Dynamically Compressible Context Architecture for Low Power Coarse-Grained Reconfigurable Array", to appear in Proceedings of *IEEE Intl. Conference on Computer Design (ICCD)*, Oct. 2007.
- [34] P. Bhojwani*, J. D. Lee* and Rabi Mahapatra, "SAPP: Scalable and Adaptable Peak Power Management in NoCs", to appear in Proceedings of *Intl. Symposium on Low Power Electronic Devices (ISLPED)*, August 2007.
- [35] P. Bhojwani* and Rabi Mahapatra, "A Robust Protocol for Concurrent On-Line Test (COLT) of NoC-based Systems-on-a-Chip", Proceedings of *ACM/IEEE Design Automation Conference (DAC)*, 2007. (Acceptance rate 25%, ~800 submissions)
- [36] P. Bhojwani* and Rabi Mahapatra, "An Infrastructure-IP for online testing of network-on-chip based SoCs", Proceedings of *IEEE Intl. Symposium for Quality Electronic Devices (ISQED)*, 2007.(Acceptance rate ~30%, 300+ submissions).
- [37] Ranjani Sridharan* and Rabi Mahapatra, "Analysis of Real-time Embedded Applications in the Presence of Stochastic Fault Model," *Proceedings of ACM/IEEE Intl. Conference on VLSI Design, 2007*.
- [38] Rupak Samanta* and Rabi Mahapatra, "An Enhanced CAM Architecture to Accelerate LZW Compression," *Proceedings of ACM/IEEE Intl. Conference on VLSI Design, 2007*.
- [39] R. Singhal*, S. Chang, G. Choi, and R. Mahapatra, "Error Control Coding for Combinatorial Circuits based on Output Delay Correlation", Accepted for *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2007.
- [40] Rohit Singhal*, Gwan Choi, and Rabi Mahapatra, "Information Theoretic Approach to Address Delay and Reliability in Long On-Chip Interconnects," *Proceedings of ACM/IEEE Intl. Conference on Computer-Aided Design (ICCAD) 2006*.
- [41] P. Bhojwani* and R. Mahapatra, "Core Network Interface Architecture and Latency Constrained On-Chip Communication", in *IEEE Symposium on Quality Electronic Design, 2006 (ISQED)*, pp.358-363 .

- [42] R. Singhal*, G. Choi and R. Mahapatra, "Information Theoretic Capacity of Long On-chip Interconnects in the Presence of Crosstalk", *Proceedings of IEEE Symposium on Quality Electronic Design, 2006 (ISQED)*, pp.407-412 (Acceptance rate 40%)
- [43] R. Singhal*, G. Choi and R. Mahapatra, "Programmable LDPC Decoder Based on the Bubble-Sort Algorithm," Accepted for Publication in *Proceedings of ACM/IEEE International Conference on VLSI Design 2006*.
- [44] D. Wu*, G. Venkataraman, J. Hu, Q. Li, and R. Mahapatra, "DiCER: Distributed and Cost-Effective Redundancy for Variation Tolerance," Accepted for Publication in *Proceedings of ACM/IEEE Intl. Conference on Computer-Aided Design (ICCAD) 2005*. (Acceptance rate 25%)
- [45] S. Ahmad* and R. Mahapatra, "TCAM Enabled On-Chip Logic Minimization", *Proceedings of ACM/IEEE Intl. Design Automation Conference (DAC) 2005*. (Acceptance rate: 20%)
- [46] A. Chousein* and R. Mahapatra, "Fully Associative Cache Partitioning with Don't Care Bits for Real-time Applications", *11th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, March 2005.
- [47] V. Rai* and R. Mahapatra, "Lifetime Modeling of a Sensor Network," *Proceedings of IEEE Intl. Conf. on Design, Automation and Test in Europe (DATE)*, March 2005. (Acceptance rate: 25%)
- [48] D. Wu*, J. Hu and R. Mahapatra, "Coupling Aware Timing Optimization and Antenna Avoidance in Layer Assignment," *Proceedings of ACM Intl. Symposium on Physical Design, (ISPD) 2005*. (Acceptance rate: 32%)
- [49] P. S. Bhojwani*, R. Mahapatra, E. J. Kim and T. Chen, "A Heuristic for Peak Power Constrained Design of Network on Chip (NoC) based Multimode Systems," *Proceedings of IEEE Intl. Conf. on VLSI Design, IEEE Computer Press*, January 2005, pp.124-129. (Acceptance rate: 27.5%)
- [50] D. Wu*, J. Hu, M. Zhao and R. Mahapatra, "Timing Driven Track Routing Considering coupling Capacitance," *Proceedings of IEEE Intl. Conference on ASP-DAC*, January 2005, pp. 1156-1159.
- [51] A. Kumar* and R. Mahapatra, "Integrated Scheduling and Buffer Management Scheme for Input Queued Switches with Extreme Traffic Conditions," *Proceedings of IEEE International Conference on Computer Communication (ICC)*, May 2005. (Acceptance rate: 34%).
- [52] S. Ahmad*, N. Jayakumar*, S. Khatri and R. Mahapatra, "X-Routing using Two Manhattan Routing Instances," Accepted for Publication in *Proceedings of IEEE International Conference on Computer Design (ICCD) 2005*.

- [53] K. Padhi* and R. Mahapatra, "A Technique for Identification of Voice in Stereo Soundtracks," Accepted for Publication in *Proceedings of IEEE International Conference on Information, Communications and Signal Processing (ICICS 2005)*
- [54] R. Singhal*, G. Choi and R. Mahapatra, "Quantized LDPC Decoder Design for Binary Symmetric Channels," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, Japan, May 23-26, 2005.
- [55] S. Ahmad* and R. Mahapatra, "m-Trie: An Efficient Approach to On-chip Logic Minimization," *Proceedings of ACM/IEEE Intl. Conference on Computer-Aided Design (ICCAD) 2004*, pp. 428-435. (Acceptance rate: 24%)
- [56] S. Choudhuri* and R. Mahapatra, "Energy Characterization of File Systems for Diskless Embedded Systems," *Proceedings of ACM /IEEE Intl. Design Automation Conference (DAC) 2004*, pp. 566-569. (Acceptance rate: 20%)
- [57] A. Rajaram*, J. Hu and R. Mahapatra, "Reduced Clock Skew Variability via Cross Links," *Proceedings of ACM/IEEE International Design Automation Conference (DAC 2004)* pp. 18-23. (Acceptance rate: 20%), (**Best Paper Nominee**)
- [58] D. Wu*, J. Hu, R. Mahapatra and M. Zhao, "Layer assignment for Crosstalk Risk Minimization," *Proceedings of IEEE Intl. Conference ASP-DAC 2004*, pp.159-162.
- [59] A. Rajaram*, W. Guo, B. Lu, R. Mahapatra and J. Hu, "Analytical Bound for Unwanted Clock Skew due to Wire Width Variation," *Proceedings of IEEE Intl. Conference on Computer-Aided Design (ICCAD) 2003*, pp. 401-407. (Acceptance rate: 25%)
- [60] P. Bhojwani* and R. Mahapatra, "Interfacing Cores with On-chip Packet-Switched Networks," 16th *IEEE International Conference on VLSI Design, Proceedings on VLSI Design*, Jan 2003, pp. 382-387 (Acceptance rate 39%)
- [61] V. C. Ravikumar*, R. Mahapatra, J.C. Liu, "Modified LC-Trie based Efficient Routing Look Up," 10th *IEEE/ACM International Conference on Modeling Analysis and Simulations of Computer & Telecommunications (MASCOTS)*, October 2002, pp. 177-182. (Acceptance rate: 30%)
- [62] A. Prasad*, W. Qui* and R. Mahapatra, "Hardware Software Partitioning of Multifunction Systems," *Proceedings of Intl. Conf. on Information Technology*, Dec 2002, pp. 35-40. (Acceptance rate: 25%)
- [63] M. Pirvu*, L. Bhuyan and R. Mahapatra, "Hierarchical Simulation of a Multiprocessor Architecture," *Proceedings of Intl. Conference on Computer Design (ICCD)*, October 2000, pp. 585-588.
- [64] B. K. Das*, R. Mahapatra and B. N. Chatterji, "Modeling of Wavelet Transform for De Bruijn Graph Connected Multiprocessors," *Proceedings of Intl. Conf. on PDPTA'97*, July 1997, pp. 1482- 1489.

- [65] S. Mahapatra* and R. Mahapatra, "Mapping of Back propagation Learning onto Distributed Memory Multiprocessors," *Intl. Conf. on Algorithms & Architectures for Parallel Processing*, Brisbane, April 1995.
- [66] C. R. Tripathy*, R. B. Misra and R. Mahapatra, "Evaluation of Fuzzy Reliability of Multistage Interconnection Networks," *Proceedings of Intl. Conf. on Automation*, India, 1995, pp. 87-91.
- [67] C. R. Tripathy*, S. Patra*, R. Mahapatra and R. B. Misra, "Reliability Modeling and Analysis of Multiprocessor Systems," *Proceedings of Intl. Conf. on Stochastic, Optimization and Computer Applications*, Coimbatore, Dec. 1994, pp.77-91.
- [68] R. Mahapatra and J. Majumdar*, "Implementation of Fast Hartley Transform on Multiple Bus Cache Coherent Multiprocessors," *Proceedings of Intl. Conf. on Parallel Distributed Systems (ICPADS)*, Taiwan, Dec. 1994.
- [69] R. Mahapatra, A. Kumar* and B. N. Chatterji, "Vector Hartley Transform Employing Multiprocessors," *Proceedings of Intl. Symposium on Parallel processing (IPPS)*, April, 1992, pp. 250-253.
- [70] R. Mahapatra and B. K. Kar*, "A Multilayered VLSI Array for Multistage Interconnection Network," *Fourth Intl. Symposium on VLSI Design*, Jan. 1991.
- [71] R. Mahapatra, V. A. Kumar*, B. K. Das and B. N. Chatterji, "Performance Analysis of Parallel FFT Algorithm on Multiprocessors," *Intl. Conference on Parallel Processing (ICPP)*, vol. III, August 1990, pp. 368-369.
- [72] R. Mahapatra, V. A. Kumar*, and B.N. Chatterji, "Performance Analysis of Fast Hartley Transform Algorithm on Multiprocessor Systems," *Intl. Symposium on Computer Architecture and Digital signal Processing*, Hong Kong, October 1989.
- [73] K. V. S. Rao, N. Adishesu, R. Mahapatra and B. K. Sarap, "Design and Development of 32-element Microstrip Dipole Conformal Array," *Intl. Symposium on Electronics, Devices and Circuits*, Kharagpur, Dec. 1987.

Book Chapters

- [74] B. K. Das*, R. Mahapatra and B. N. Chatterji, "Modeling of Wavelet Transform on Multiprocessor Systems," *IT: Challenges and Opportunities*, Tata McGraw Hill Publication, Nov.1995, pp. 335-346.
- [75] B. K. Das*, R. Mahapatra, "An Efficient Circle Detection Scheme using a Two Dimensional Array of Accumulators," *Pattern Recognition, Image Processing and Computer Vision: Recent Advances*, Narosa Publishing House, New Delhi, 1995, pp. 230-237.

- [76] V. A. Kumar*, B. K. Das* and R. Mahapatra, "Performance Analysis of Hough Transform on Parallel Architectures," *Frontiers in Parallel Computing*, Narosa Publishers, 1990, pp. 279-288.

Peer Reviewed Workshop

- [77] A. Biswas and R. Mahapatra, "Managing Confidence and Reliability in Complex Software Systems with an Adaptive System Monitor", *NSF Workshop on High-Confidence Software Platforms for Cyber-Physical Systems (HCSP-CPS)*, Virginia , Nov 2006.
- [78] P. Bhojwani, R. Singhal, G. Choi, R. Mahapatra, "Forward Error Correction for On-chip Interconnection Networks", *Proceedings of International Workshop on Unique Chips and Systems (UCAS-II)* 2006.
- [79] M. Nolan and R. Mahapatra, "A TDM Test Scheduling Method for Network-on-Chip Systems," to be presented in *IEEE International Workshop on Microprocessor Verification & Testing (MTV)* 2005.
- [80] H. Kim*, E. J. Kim and R. Mahapatra, "Power Management in RAID Server Disk System Using Multiple Idle States," *Proceedings of International Workshop on Unique Chips and Systems (UCAS)* March 2005.
- [81] N. Goyal* and R. Mahapatra "Energy Characterization of Cramfs for Embedded Systems," *International Workshop on Software Support for Portable Storage (IWSSPS)*, March 2005.
- [82] K. Pramod* and R. Mahapatra, "PAP: Power Aware Partitioning of Reconfigurable Systems," *Proceedings of HPCA Workshop on Software Support for Reconfigurable System (SSRS)*, Anaheim, CA, February 2003, pp. 39-45.
- [83] M. Satpathy, R. Mahapatra, S Choudhuri* and S. V. Chintis, "High Performance Code Generation through Lazy Activation Records," *Proceedings of IEEE Workshop on Interaction between Compilers and Computer Architecture (INTERACT 7)*, IEEE Computer Press, February 2003, pp. 37-50.
- [84] N. Subramanian*, S. Pandita* and R. Mahapatra, "Co-Design of Reactive Embedded System for Motion Control in Hostile Environment," *Proceedings of 8th IAPR workshop on Machine Vision Applications*, Japan, December 2002.
- [85] D. Mohanty*, Rabi Mahapatra and Gwan Choi, "A Design Space Exploration Framework in Multiprocessor SoC Codesign," *Proceedings of IEEE Workshop on Embedded Systems*, Dec 3, 2001.
- [86] B. K. Das*, R. Mahapatra and B. N. Chatterji, "Modeling of Wavelet Transform on Multistage Interconnection Network," *Second Conference on Parallel and Real-Time Systems*, Perth, September 1995.

- [87] C. R. Tripathy*, R. Mahapatra and R. B. Misra, "Reliability Evaluation of MIN by Network Decomposition," *First Intl. Workshop on Parallel Processing*, Bangalore, pp. 228-233, Dec. 1994.
- [88] B. K. Das*, R. Mahapatra and B. N. Chatterji, "Design of Multiprocessor Based Image Tracker," *IEEE Conf. on Microprocessor Application on Industrial Instrumentation Systems*, Bhubaneswar, August 1994.
- [89] R. Mahapatra and J. Majumdar*, "Modeling FCT Algorithm on MBCC Multiprocessors," *Indo-US Workshop*, Pune, Dec. 1993.
- [90] C. R. Tripathy*, R. B. Misra and R. Mahapatra, "An efficient method to evaluate reliability of multistage interconnection networks," *Proc. Natl. Seminar on Information Technology*, Itanagar, India, pp. 1-7, 1993.
- [91] R. Mahapatra and B. K. Kar*, "A Systolic Design of Benes and Data Manipulator Network for VLSI Implementation," *Third Intl. Workshop on VLSI Design*, pp. 275-282, Jan.1990
- [92] R. Mahapatra, B. K. Das*, V. A. Kumar* and B. N. Chatterji, "Performance of 2D IFCT Algorithm on Multiprocessors," *Proc. Workshop on Parallel Processing*, BARC, Bombay, Feb.1990.
- [93] L. K. Dash*, R. Mahapatra and B. N. Chatterji, "An Efficient Hardware Scheme for Computing Histogram," *Intl. Seminar on Frontiers in Imaging*, Trivandrum, July 1990.

Technical Reports

1. Damian Dechev*, Rabi Mahapatra, Bjarne Stroustrup, "Chocolate: Class Hierarchies for Optimizations of Compiler Algorithms", Department of Computer Science Technical Report #TR-CS-2005-01, Texas A&M University, <http://students.cs.tamu.edu/d0d1973/>
2. Anuj Kumar* and Rabi Mahapatra, "Enhancing TLB Reach using TCAM Cells", Technical Report # TR-CS-2005-03-01
3. Junyi Ling* and Rabi N. Mahapatra, "A Graphic Architecture for Ray Tracing and Photon Mapping", Technical Report # TR-CS-2004-01-0
4. John Wisinger* and Rabi Mahapatra, "FPGA Based Image Processing with the Curvelet Transform", Technical Report # TR CS-2003-01-0
5. Rabi N Mahapatra and Brian Murray*, "GEARS: Graphics Embedded Accelerated Rendering Systems: Development of an Embedded 3D Graphic Processor", Technical Report # TR-CS-2002-05-1
6. Vinod Raman*, Pankaj Bhagwat* and Rabi Mahapatra, "An Efficient Implementation of IS-95 CDMA Reverse Link Transceiver: A Codesign Approach", TR# TR-CS-2002-05-2
7. Rajesh Prathipati* and Rabi Mahapatra, "A Three Step Approach For Low Power Static Scheduling Of Real-Time Embedded Systems" Technical Report # TR-CS-2002-06-0

8. Di Wu* and Rabi Mahapatra, “Multiprocessor Based Voltage Scaling: A Low-Power Technique”, Technical Report # TR-CS-2002-06-1
9. Raman Senthil Kumar*, Bhamy Madhava Shenoy* and Rabi Mahapatra, “Optimizing Power at the Physical Layer in a Wireless Ad Hoc Network”, TR# TR-CS-2002-06-2
10. Narayanan Swaminathan* and Rabi Mahapatra, “Communication Architecture Synthesis of Packet-Switched Network-on-Chip”, Technical Report # TR-CS-2002-08-0
11. Sunil Bhosekar* and Rabi Mahapatra, “Estimating Cache & TLB Power in Embedded Processor Using Complete Machine Simulation”, Technical Report # TR-CS-2001-08-0

Invited Talks

1. Brighten-up TLB/Cache Architecture with Blind Bits, *IEEE Section Lecture*, Indian Institute of Technology, Kharagpur; January 14, 2005.
2. Hardware-Software Codesign of Embedded Systems, *Invited Talk in Intl. Symposium on Technocatalyst*, Orissa, India, January 8, 2005.
3. Brighten up Your Cache Architecture with Blind Bits, *Intel Research Lab*, Santa Clara, CA; November 2004.
4. m-Trie for on-chip Logic Minimization, Router Architecture Group at CISCO, CA, November 2004.
5. Exploiting slacks in distributed embedded systems, Graduate Seminar in computer Science, Texas A&M University, September 2004.
6. Energy efficient File System Management for Embedded Systems, IBM Austin, February 2004.
7. TCAM based Router Architecture for IP lookup”, *Departmental Seminar*, Computer Science, University of California, Riverside, November 21, 2003.
8. A Comprehensive Codesign Framework for Embedded Systems, *Departmental seminar*, Faculty & graduate Students, Computer Science, University of Maryland at Baltimore County, Baltimore, MD, May 2001.
9. Hardware-Software Codesign for Embedded Systems, Department of Electrical Engineering, Oklahoma State University, Hartford University, and Michigan Tech University, April 2001.
10. Design Challenges in Embedded Systems, KIIT Deemed University, India, June 2000.
11. Reconfigurable Computing: A case for Digital Signal Processing, *Departmental seminar*, Faculty & Students, ECE Dept., Utah State University, Logan, UT, December 99.
12. Trends on Reconfigurable Computing, *Departmental seminar*, Faculty & Students, CS Dept., University of South West Texas, San Marcus, TX, June 1999.

Professional Honors, Awards and Membership

- Ford Fellow, Texas A&M University, 2001.

- Senior Member, IEEE Computer Society: Since 1994.
- Indo-US Young Scientist Award: BOYS-CAST Fellow 1987 in the area of Parallel Processing by Department of Science & Technology, Government of India.
- Member, ASEE

Teaching

Courses Taught at TAMU since Fall 2001

Spring 2005: Hardware Software Codesign for Embedded Systems (CPSC 617)
Fall 2004: Computer System Design (Capstone Senior Design) CPSC 483.
Spring 2004: Computer Architecture (CPSC 321); Embedded Systems (CPSC 689)
Fall 2003: Computer System Design (CPSC 483)
Spring 2003: Embedded System Codesign (CPSC 689)
Fall 2002: Computer System Design (CPSC 483)
Spring 2002: Computer System Design (CPSC 483) and
Hardware-Software Codesign of Embedded System (CPSC 689),
Fall 2001: Computer System Design (CPSC 483)

Under Graduate Courses Taught

Hardware-Software Codesign of Embedded Systems (CPSC 489), Computer Architecture (CPSC 321), Operating Systems, Data Structures (CPSC 210), Digital System design (ELEN 248), Microcomputer Systems (CPSC 462), Computer System design (CPSC 483), Switching & Automata Theory, and Advanced Computer Architecture.

Graduate Courses Taught

Hardware-Software Codesign of Embedded Systems Spring (CPSC 689/617), Advanced Computer Architectures (CPSC 614), Parallel & Distributed Processing, Design and Analysis of Algorithms, Advanced Operating System Design, Fault Tolerant Computing, and Selected Topics on Computer Engineering.

Student Evaluation Ratings: On average more than 4.2 in the scale of 5.0 for both graduate and undergraduate courses.

Graduate Students Advising

Ph.D. Students Graduated (Current Position)

1. B. K. Das, Ph.D. 1995, Student at IIT Kharagpur, Title: *Modeling of Some Image Processing Transforms for Multiprocessor Architecture*, (Deputy Director, Defense Research Development Organization, India).
2. Sudipta Mohapatra, Ph.D. 1996, Student at IIT Kharagpur, Title: *Some Studies on Mapping of Neural Network Models onto Parallel Architectures*”, (Asst. Professor, Indian Institute of Technology, Kharagpur).

3. C. R. Tripathy Ph.D.1996, Student at IIT Kharagpur, Title: *Dependability Analysis of Parallel Computer Interconnection Networks*, (Professor, Computer Science & Engineering, Sambalpur University).

Current Ph.D. Students, Topics (Expected Completion Date)

4. Di Wu, "*Layer Assignment in Deep Sub-micron Technology*" (Current Position: Staff Engineer, Cadence Ltd, San Jose, CA, since June 2005), (Thesis defense - October 10, 2005, Co-chair: Jiang Hu, EE).
5. Praveen Bhojwani, "*Communication Synthesis in Network on Chip*" (Fall 2006)
6. Rohit Singhal, "*Reliable and Low-power On-chip Interconnect*" (Fall 2006, Co-Chair: Gwan Choi, EE)
7. Rupak Samanta, "*TCAM Enable Cache Architecture for Low-power*" (Fall 2007)
8. Ali Chousein, "*Efficient Cache Architecture for Real-time Embedded Systems*" (Fall 2007)
9. Kabi P. Padhi, "*Energy Efficient Sensor Networks*" (Fall 2007)
10. Ranjani Sridharan, "*Optimization issues in NanoCMOS Design*", (Fall 2007)
11. T. S. Kim, "*Low-Power Real-time Embedded Systems*", (Spring 2008)
12. Jason Lee, "*Efficient Logic Synthesis in ASIPs*", (Fall 2008)

MS Students Thesis Advising (Chair) at Texas A&M with their Current Employer

1. Seraj Ahmad, "*High Performance IP Lookup Architecture for Network Routers*", Fall 2005.
2. Jason Surprise, "*An Energy Efficient TCAM Enhanced Cache Architecture*", Fall 2004; (Raytheon)
3. Nitesh Kumar, "*Macro-Modeling and Energy Efficiency Studies of File Management in Embedded Systems with Flash Memory*", Fall 2004; (Amazon).
4. Anuj Kumar, "*TCAM Enabled TLB Architecture*", August 2004; (Microsoft)
5. Subrata Acharya, "*Dynamic Slack Management in Real-time Distributed Embedded Systems*", August 2004; (Ph.D. Student at University of Pittsburgh).
6. Anand Rajaram, "*Analytical Bound for Unwanted Clock Skew due to Wire Width Variation*", May 2004 (Co-Chair: Jiang Hu); (Texas Instruments)
7. Junyi Ling, "*A Graphic Architecture for Ray Tracing and Photon Mapping*", May 2004; (Ph.D. Student at University of California, Irvine).
8. Ravikumar V. C, "*An Energy Efficient TCAM based Router Architecture*", December 2003; (Hewlett Packard)
9. Rajesh Prathipati, "*Energy Efficient Slack Distribution Technique in Real-Time Embedded Systems*", December 2003.
10. Praveen Bhojwani, "*Synthesis of Interfaces in Network on Chip*", August 2003; (Ph.D. Student at TAMU).
11. Siddhartha Choudhuri, "*Energy Characterization and Analysis of File Systems for Diskless Embedded Systems*", August 2003, (Ph.D. student at Univ. of California, Irvine).

12. Vijay Rama Pramod K, “*PAP: Power Aware Partitioning of Reconfigurable System*”, December 2002, (Co-Chair: A N Reddy).
13. John Wisinger, “*FPGA Based Image Processing Accelerators*”, December 2002; (INVOCON Inc, Houston).
14. Narayanan Swaminathan, “*Communication synthesis of On Chip Network*”, August 2002; (Texas Instruments).
15. Brian Murray, “*Development of a 3D Embedded Graphic Processor*”, May 2002; (Motorola, Austin).
16. Sunil Bhosekar, “*Architecture-Level Power Estimation & Optimization using a Complete Simulator*”, December 2001; (Dallas Semiconductor Ltd.).
17. Rahul Katoria, “*A Power-Aware Partitioning of HW-SW Codesign*”, August 2001 (Intel).
18. Srikant Kasturi, “*An Optimized Data Link Layer*”, May 2001, Co-Chair: A N Reddy; (Hewlett Packard).

Undergraduate Student Research Mentoring

- Stephen Hansen, NSF REU Fellow (Summer 2004), University Research Fellow (Fall 2004-Spring 2005); *Honorable Mention in the CRA's Outstanding Undergraduate National Award for 2004*.
- Allen Parish, Undergraduate Research Scholar (Fall 2004 - Spring 2005).
- Amarachi Okorie, Engineering Scholar Program (Spring 2002) and Summer Research Fellow 2002.

Professional Services

Panelist & Outside Reviewer

- NSF Panel, Medium ITR, Computer Communication Research Program, May 2002.
- NSF proposals for regular CCR Program 1999, 2001
- SERC proposal, 12/99;

Conference Activities

Program Chair, Workshop on Embedded System Codesign, ESCODES 2002.
Steering Committee Chair: Intl. Conference on Information Technology, 2004, 2005.

Member of Program Committee

Recent Events

- Technical Program Committee Member, 42nd IEEE/ACM Design Automation Conference (DAC) 2005-2007.
- IEEE Second Workshop on High Performance, Fault Adaptive, Large Scale Embedded Real-Time Systems (FALSE 2005).

- International Workshop on Embedded Real-Time Systems Implementation (ERTSI) 2004.
- First International Workshop on Network of Embedded Computing (NEC) 2004.
- Intl. Workshop on Large Scale Real-Time Embedded System (LARTES) 2002, 2003.
- International Conference on Parallel Processing (ICPP) 2004,
- International Conference on Parallel & Distributed Systems (ICPADS) 2004,

Other Events

- *Program Committee Member:* Workshop on Embedded systems 2001, ADCOMP98, Parallel & Distributed Processing Techniques and Applications (PDPTA97), PDPTA98, PDPTA99, Image Science System Technology (CISST99), Advanced Computing & Communication (ADCOMP) 1997
- *Session Chairs:* Intl. Conference on Information Technology, (CIT 2002), IEEE Real-Time Systems Symposium, September 2002, IEEE Real Time Application Symposium (RTAS 2002), December 2002, PDPTA97, ADCOMP97, etc.
- *International Conference Reviewer:* ACM/IEEE Design Automation Conference 2005, IEEE Intl. Conf. on VLSI Design 2003, Intl. Conf. on Computer Aided-Design (ICCAD) 2002, Workshop on Large Scale Real-Time and Embedded Systems (LARTES) 2002, Infocom 2004, ICPP 2004, ICPADS 2004, etc.
- *Vice General Chair,* International Conference on Information Technology, Dec. 20-22, 1999, India.
- *Program Chair,* Intl. Conference on Information Technology, (CIT'98), Dec.21-23, 1998, India
- *Program Chair,* IEEE Conference on Parallel and Distributed Systems, July 13-14, 1993, Kharagpur, India.

Chair Elected and Served

- Chairman, IEEE Section, Kharagpur, 1994 - 1995
- Vice Chairman, IEEE Section, Kharagpur, 1993 -1994

Panel Member

- Panel on *Research and Development of Parallel and Distributed Computers in Asian Countries*, Intl. Conference on Parallel and Distributed Systems - Dec.19-21, 1994, Hsinchu, Taiwan.

International Journal Reviewer

- IEEE Transactions on Computers
- IEEE Transactions on Parallel and Distributed Systems
- ACM Transactions on Design Automation of Embedded Systems
- IEEE Transactions on Circuits and Systems II
- IEEE/ACM Transactions on Networking
- IEEE Transactions on Computer Aided Design

- Journal of Parallel & Distributed Computing (JPDC)
- IEEE Transaction on Signal Processing
- IEEE Communication Letters
- Signal Processing Journal
- Microelectronics Journal
- Parallel Computing
- Parallel Processing Letters

Departmental Service

- Graduate Students Admission Committee, 1999, 2001 - present
- REU (NSF) Faculty Committee 2004-2006.
- ABET Committee, Department of Computer Science, 1997- 2004
- Graduate Administration Committee, 2001- 2002
- Faculty Award Committee, 2001- 2002.
- Computer Services Advisory Committee, 1997- 2001.
- Colloquium Committee, 2001- 2002
- Graduate Advisor, Computer Engineering, Program, Indian Institute of Technology, Kharagpur, Fall'93 – Summer 95.
- Faculty Advisor, Under Graduate, E&ECE Dept., Indian Institute of Technology, Kharagpur, Fall'92 - Spring' 94