# CROWNE: Current Ratio Outliers With Neighbor Estimator

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***Abstract***

*Increased leakage and process variations make distinction between fault-free and faulty chips by $I_{DDQ}$ test difficult. Earlier the concept of Current Ratios (CR) was proposed to screen defective (outlier) chips. However, it is not capable of catching certain defects. Neighboring chips on a wafer have similar fault-free parameters that are correlated through the underlying fabrication process. Based on this observation, an alternative test metric called Neighbor Current Ratio (NCR) was proposed. NCR screens outlier chips based on their nonconformance to local variation in $I_{DDQ}$. In this paper, we explore the correlation between different vectors that yield CR and NCR values. The effectiveness of NCR along with additional test parameters to screen outlier chips is evaluated using industrial test data.*

## 1. Introduction

As advances in technology permit shrinking of device geometries test engineers face new challenges [1]. Leakage current ($I_{DDQ}$) testing is capable of detecting certain unique defects that can lead to low reliability [2] [3]. It is based on the premise that fault-free chips have smaller leakage current than faulty chips. However, for deep sub-micron chips fault-free leakage current increases and distinction between faulty and fault-free currents becomes fuzzy [4] making the future of $I_{DDQ}$ test uncertain. The conventional single pass/fail threshold method results in unjustifiable yield loss. This makes $I_{DDQ}$ pass/fail threshold setting a difficult challenge.

$I_{DDQ}$ test data shows a continuous distribution with outlier (defective) chips in the tail. Several solutions have been proposed in the literature to extend $I_{DDQ}$ test to deep sub-micron (DSM) technologies by reducing variance in the data using graphical means [5] or statistical post-processing of data [6][7]. Most of these methods rely on the observation that variations in fault-free $I_{DDQ}$ are regular and deterministic and those caused by a defect are random in nature. Current Ratio (CR) is easy to implement in production. However, CR threshold setting is difficult due to variation in CRs [8]. It is observed that CR cannot effectively screen certain outlier chips that pose a reliability risk and may result in customer returns. Since it can impact quality, screening such chips is vitally important. Any parameter variation that cannot be explained by a defect-free mechanism, is due to a defect. Hence, it is suggested that *being different* is reason enough for suspecting and/or rejecting chips even if they pass all functional tests. Although this results in "apparent" yield loss, it should improve outgoing quality. One way to conclusively determine this is to compare burn-in results with the predicted chip behavior (pass/fail). Obviously such extrapolations are not possible when no burn-in (BI) data is available.

The goal of this paper is to use multiple test metrics for outlier chips. The remainder of this paper is structured as follows. In the next section, we describe CR concept and its limitations. Using industrial test data, we illustrate that certain defective chips can have nominal CR. In Section 3, we review Neighbor Current Ratio (NCR) metric to find outliers and explore the relationship between different vector pairs used for CR/NCR computation. Section 4 illustrates the use of multiple test metrics for outlier rejection. Section 5 outlines the analysis methodology. Section 6 discusses the experimental results and finally Section 7 concludes the paper.

## 2. Current Ratio and Process Variability

The current Ratio of a chip is the ratio of the maximum $I_{DDQ}$ to the minimum $I_{DDQ}$ [6]. It is based on the observation that the intra-die (within-die) variation in $I_{DDQ}$ for fault-free chips is deterministic and relatively constant. That is, a fault-free chip that leaks more does so for all vectors. The presence of an active (pattern-dependent) defect violates this assumption, resulting in higher than nominal CR. The nominal CR is determined by characterization.

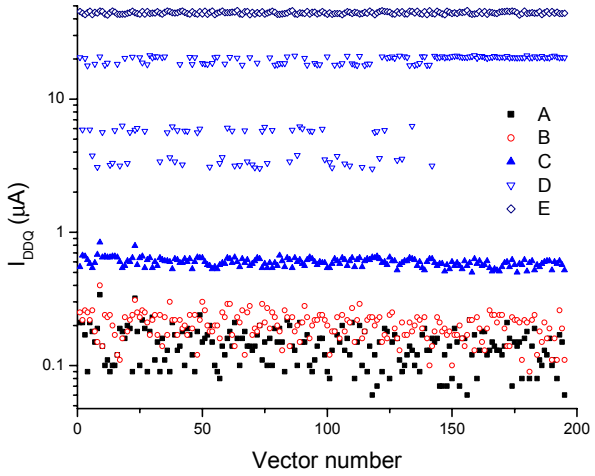


**Fig. 1. Five dice showing variation in $I_{DDQ}$.**

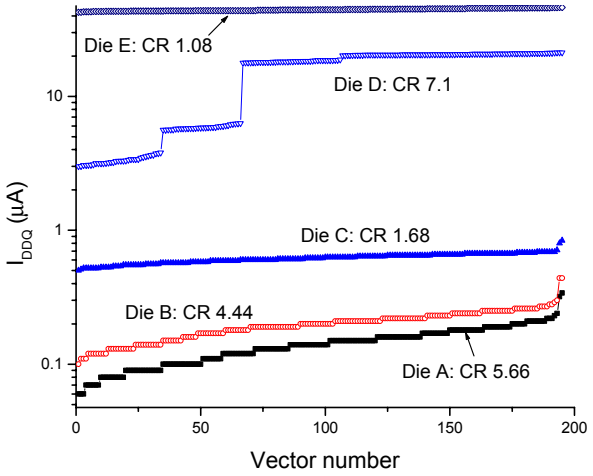


**Fig. 2. Current signatures for dice shown in Fig.1.**

Variability is inevitable for semiconductor processes due to changes in processing conditions and is reflected in test parameters of chips. For example, leakage current values vary from chip to chip for identical vectors. An example illustrating this is shown in Fig. 1 using five dice labeled 'A' through 'E'. Their min, max and mean $I_{DDQ}$ values, intra-die standard deviation in $I_{DDQ}$ and CRs are tabulated in Table 1. Fig. 2 shows the current signatures for these dice. In Fig. 2 the vector-to-vector order is lost due to sorting. Fig. 2 clearly shows that a small CR does not necessarily mean a defect-free chip (Dice *C* and *E*) and defective (Die *D*) as well as fault-free chips can have high CR (Dice *A* and *B*). For a defective chip, high CR is obtained only if at least one vector does *not* excite the defect and the defective current is higher than the nominal current (for vectors that excite the defect). If all vectors excite the defect (passive or multiple defects with similar defect currents excited by different complementary set of vectors), CR actually reduces with increasing defect current as shown in Fig. 3. To screen defective chips having low CR, additional test information must be used. We proposed a metric using wafer-level spatial information that is reviewed in the next section.

## 3. Neighbor Current Ratio

Process conditions change smoothly across a wafer. Hence, for the same vector, two fault-free adjacent dice on a wafer are expected to have similar $I_{DDQ}$ (see Fig. 4). The Neighbor Current Ratio (NCR) metric is based on this observation. NCR is obtained by taking the ratio of $I_{DDQ}$ values of a die and its functional (Boolean test pass) neighbor for the *same* vector. There are eight adjacent dice for a non-edge die (Fig. 6). Ideally (for fault-free chips under no process variations), NCR is equal to 1. However, owing to process variations NCR values do vary. Dice having no immediate neighbors are ignored. With *N* functional neighbors and *k* vectors, *Nk* NCR values can be obtained. The maximum of these values is considered for outlier screening as it represents the maximum nonconformity of a chip to its spatial neighborhood. Henceforth NCR refers to the maximum NCR obtained. Fig. 5 shows the variation in NCR values across the wafer shown in Fig. 4. Notice that many spatial outliers are visible. The fault-free dice form a cluster (0.5<NCR<2.5) near the center of the wafer while some dice are obvious outliers (NCR>100). CR considers intra-die variance alone while inter-die variance is implicit through characterization. NCR on the other hand compares intra-die variation with inter-die variation.

### *Exploring the CR/NCR Vector Relationship*

There is a strong motivation for reducing the number of test vectors for increasing test efficiency. The defect screening resolution of a CR-based approach is constrained by the number of test vectors. In a production implementation of CR, $I_{DDQ}$ is measured for the "minimum $I_{DDQ}$ vector" and a limit is set on other vectors so as not to exceed the fault-free CR. Usually several vectors may fall in this category and one of them may be selected through simulation or characterization [6]. We observed which vector-pair resulted in minimum/maximum $I_{DDQ}$ (CR) for each die and which vector-pair (same vector different die) resulted in maximum NCR. Figs. 7 through 9 show histograms for 195 vectors for the SEMATECH data. Minimum $I_{DDQ}$ is mostly due to intrinsic leakage. Which vector causes minimum $I_{DDQ}$ depends on which and how many paths are turned ON/OFF. As Fig. 7 shows, vectors #9 and #23 keep the device in the minimum $I_{DDQ}$ state 75% of the time (9423 of 12128 dice). The vectors that put the device in the high $I_{DDQ}$ state are possible candidates for the maximum $I_{DDQ}$ vector. A large component of the maximum $I_{DDQ}$ is likely to be due to defective current. Due to the random nature of defects, it is unlikely to find a single vector always having the maximum $I_{DDQ}$. As Fig. 8 shows, vectors #129 and #147 most frequently have the maximum $I_{DDQ}$, but still account for less than 10% of the chips (1056 of 12128 die).

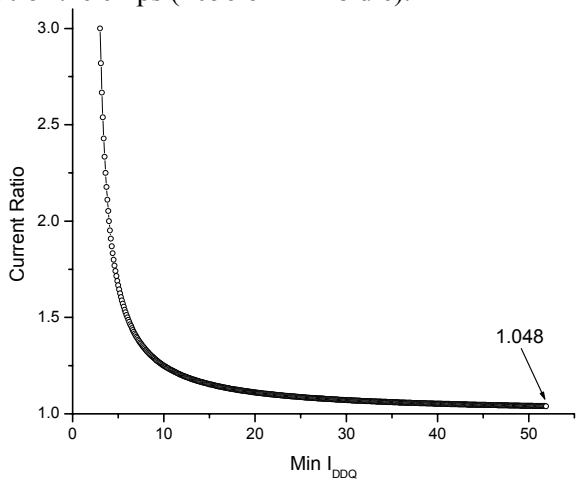


**Fig. 3. CR change with defect current.**

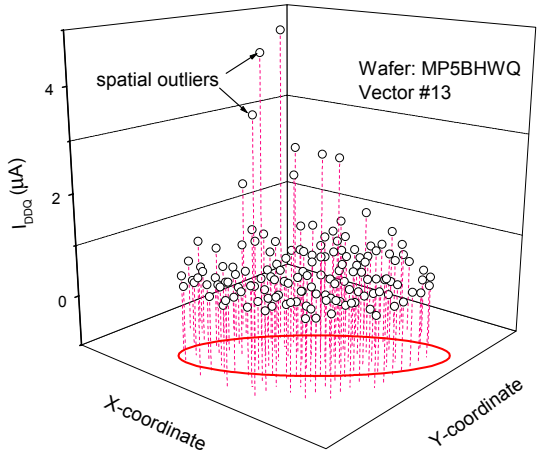


**Fig. 4. Wafer-level variation in $I_{DDQ}$.**

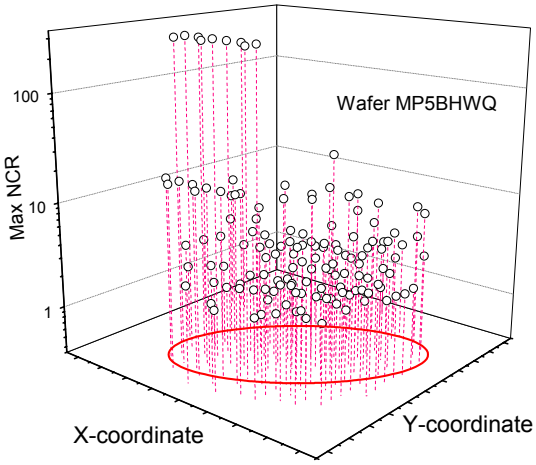


**Fig. 5. NCR variation across a wafer.**

**Table 1. Variation in CR for different dice**

| Die | Min. $I_{DDQ}$ (µA) | Max. $I_{DDQ}$ (µA) | Mean (µA) | STD (µA) | CR |
|---|---|---|---|---|---|
| Die A | 0.06 | 0.34 | 0.17 | 0.042 | 5.66 |
| Die B | 0.10 | 0.44 | 0.20 | 0.050 | 4.44 |
| Die C | 0.50 | 0.84 | 0.62 | 0.052 | 1.68 |
| Die D | 3.00 | 21.30 | 14.73 | 7.37 | 7.10 |
| Die E | 42.60 | 46.20 | 44.40 | 0.88 | 1.08 |

| | | |
|---|---|---|
| N1 | N2 | N3 |
| N4 | | N5 |
| N6 | N7 | N8 |

**Fig. 6. Neighborhood die definition.**

Since a large portion of maximum $I_{DDQ}$ stems from defect current and NCR is a *defect-oriented metric*, one would expect the vector causing maximum $I_{DDQ}$ also to result in maximum NCR. However, this need not always be true. NCR depends on which vector excites the defect for the center die and the relative magnitude

of defect current compared to neighboring die for that vector (assuming at least one neighboring die is fault-free and/or this vector does not excite a defect in a neighboring die). In general, which of the high $I_{DDQ}$ vectors results in the highest NCR depends on the defect-free behavior of the neighboring dice. As Figs. 8 and 9 show, maximum CR vector and NCR vector distributions are not always in agreement. For example, although the vector (#129) causing maximum $I_{DDQ}$ most of the time is also the vector that results in the highest NCR most of the time, this is not true for other vectors. Thus, the second most common maximum $I_{DDQ}$ vector (#147) is not the second most common maximum NCR vector (#174). Due to the random nature of defects, each vector has a potential to excite a defect, although a vector that keeps the device already in a high $I_{DDQ}$ state is more likely to result in high NCR. Selecting a single "minimum" $I_{DDQ}$ vector and setting thresholds on maximum $I_{DDQ}$ using CR, can result in yield loss as shown by Figs. 7 and 8. Although it is possible to reduce the vector set when using the NCR metric, we use the complete vector set in this work.

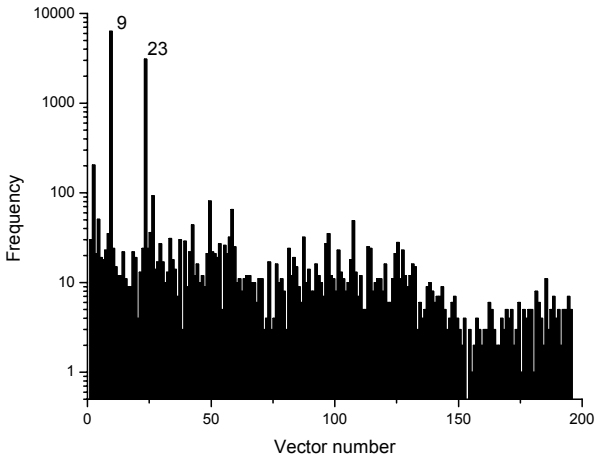


**Fig. 7. Histograms of vectors resulting in min $I_{DDQ}$.**

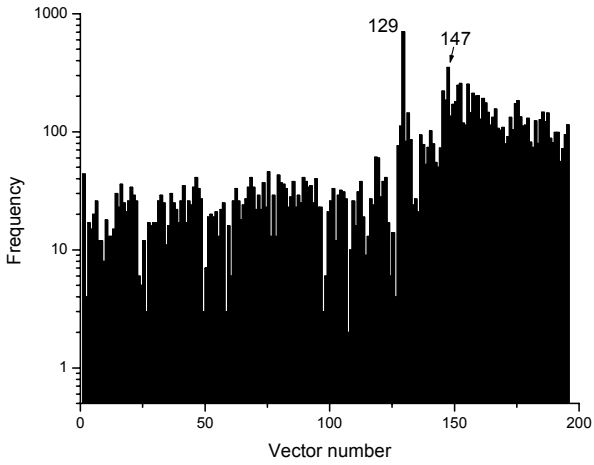


**Fig. 8. Histogram of vectors resulting in max $I_{DDQ}$**

## 4. Use of Multiple Test Metrics

As test methods begin to lose resolution, the distinction between true outliers (defective chips) and apparent outliers becomes fuzzy. The combination of multiple test metrics can be useful to screen outlier chips [9]. Earlier we showed that a combination of CR and NCR metrics can reveal certain outlier chips not caught by a single metric [10]. In the present work, we are interested in analyzing the combination of three different test metrics/parameters: CR, NCR and chip speed. The chip speed parameter could be flush delay or a test structure measurement. For example, Fig. 10 shows a scatter plot of CR and NCR values for SEMATECH chips that passed all wafer tests or failed only the 5 µA $I_{DDQ}$ test ($I_{DDQ}$<100 µA). Long tails due to outliers are visible in both X and Y directions. The chips having CR>100 and NCR>100 are obvious outliers. For screening them, a single metric is enough. However, several NCR outliers have nominal CR values (~2). Moreover, notice that a few nominal-NCR chips are CR outliers. This may occur due to defect clustering. NCR alone is not capable of screening these chips. It is observed that the distribution of chips with small CR values is very steep and outlier identification is extremely difficult. For example, in Fig. 10 deciding whether 'A' and 'B' are "true" outliers or "apparent" outliers is not straightforward. One solution is to consider additional test data to improve the confidence. Fig. 11 shows a 3D scatter plot by adding flush delay data and limiting the CR/NCR range to 10. The projection on the XY plane corresponds to the scatter plot in Fig. 10 within the range CR<10, NCR<10.

The flush delay is obtained by turning on all scan clocks so that scan flip-flops appear as a long chain of buffers and is used for speed binning. A chip that leaks more due to systematic process variation (e.g. smaller $L_{eff}$), would exhibit nominal/low CR with low flush delay. Since neighboring chips also undergo similar processing, NCR is also expected to be nominal. Similar reasoning can be applied to classify chips in different categories as shown in Table 2. Note that there are several other factors that can result in variation in one or

more test metrics. Table 2 is for illustrative purpose only. Additional test data for outlier analysis can either improve the confidence in outlier detection or explain "seemingly" outlier behavior. In addition, some outliers that are not previously visible can be identified. For example, the chip marked 'outlier' in Fig. 11, has nominal CR (4.1) and NCR (2.7) values. However, it is an outlier when flush delay (511 ns) is considered (see Fig. 13 for flush delay distribution) as it is too slow when compared to other chips having similar CR and NCR values. Chip 'A' that appears to have high CR and NCR values also has small flush delay. Clearly, this chip does not come from a fast wafer region. Chip 'B' on the other hand has nominal CR and small flush delay. Its small NCR value indicates that it comes from the fast region of the wafer.

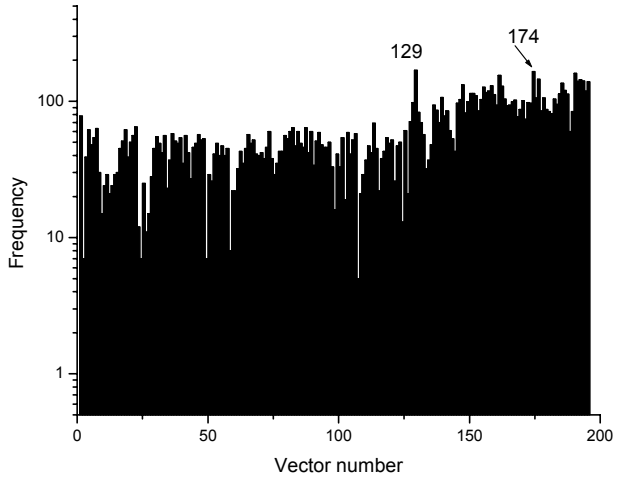


**Fig. 9. Histogram of vectors for in max NCR.**

**Table 2. CR, NCR, and delay values and chip characteristics**

| CR | NCR | Delay | Comments |
|---|---|---|---|
| Low | Low | Small | Fast wafer region |
| | | Large | Resistive short/defective? |
| Low | High | Small | A chip with passive defect in good neighborhood |
| | | Large | |
| High | Low | Small | A chip with an active defect in bad neighborhood (cluster) |
| | | Large | |
| High | High | Small | A chip with an active defect in good neighborhood |
| | | Large | |

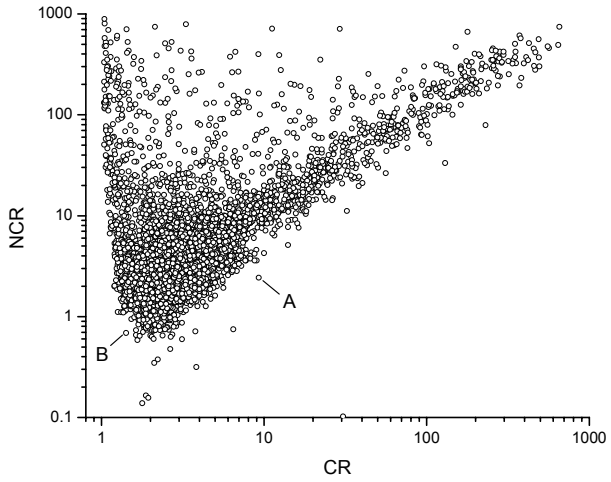


**Fig. 10. CR-NCR scatter plot for chips that passed all wafer tests or failed only $I_{DDQ}$ test ($I_{DDQ}$<100μA).**

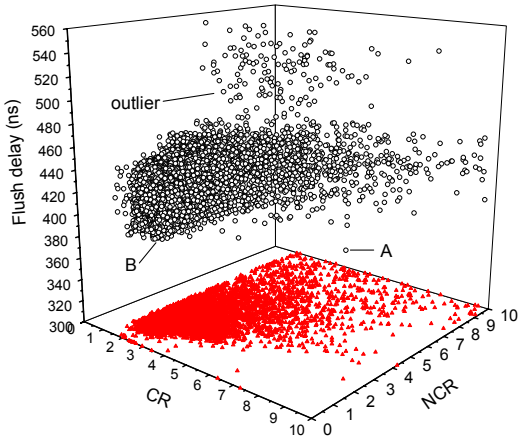


**Fig. 11. CR, NCR and flush delay scatter plot for chips having CR≤10 and NCR≤10.**

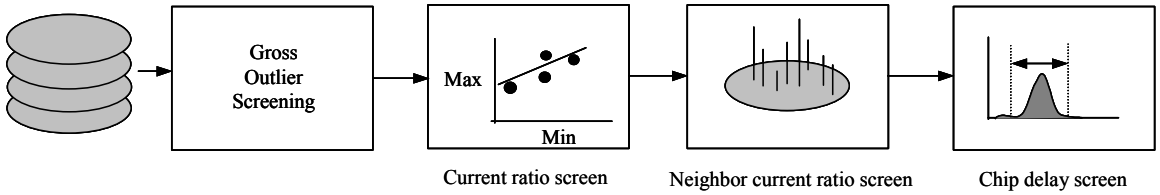


**Fig. 12. Analysis flow.**

## 5. Analysis Methodology

We use CR and NCR for outlier rejection and then use delay measurement for further screening. The analysis is carried out using wafer test data. Boolean fails are screened as their parametric test data is not reliable. We also screen gross outliers. The threshold for gross outlier rejection is obtained from cumulative distribution of test data. We used a 100 μA limit for gross outlier screening [11]. These chips are gross outliers and pose a reliability risk even if they pass all functional tests. The CR is obtained by taking the ratio of the maximum and minimum $I_{DDQ}$ values for each chip. The chips are further screened using NCR values. Chip delay data (flush delay or test circuit measurement data) distribution is used for further screening. A flush delay threshold of 500 ns is used. The analysis flow is as shown in Fig. 12.

**Table 3. Distribution of chips according to their wafer probe and post BI test results (12521 chips)**

| Wafer probe | Post BI | CR ≤5 | | CR>5 | |
|---|---|---|---|---|---|
| | | NCR ≤10 | NCR >10 | NCR ≤10 | NCR >10 |
| AP | AP | 968 | 28 | 32 | 27 |
| | IF | 20 | 2 | 2 | 3 |
| | DF | - | - | - | - |
| | IDF | - | - | - | - |
| | BF | 19 | - | - | - |
| | NB | 9552 | 126 | 254 | 198 |
| ID or IDF or DF | AP | 196 | 80 | 89 | 125 |
| | IF | 29 | 207 | 4 | 372 |
| | DF | 2 | 8 | 3 | 8 |
| | IDF | 1 | 2 | - | 3 |
| | BF | 12 | 11 | 7 | 12 |
| | NB | 45 | 28 | 3 | 43 |
| AP: All Pass, IF: $I_{DDQ}$ Fail, DF: Delay Fail, IDF: $I_{DDQ}$ + Delay Fail, BF: Voltage (Boolean) Fail NB: No Burn-in | | | | | |

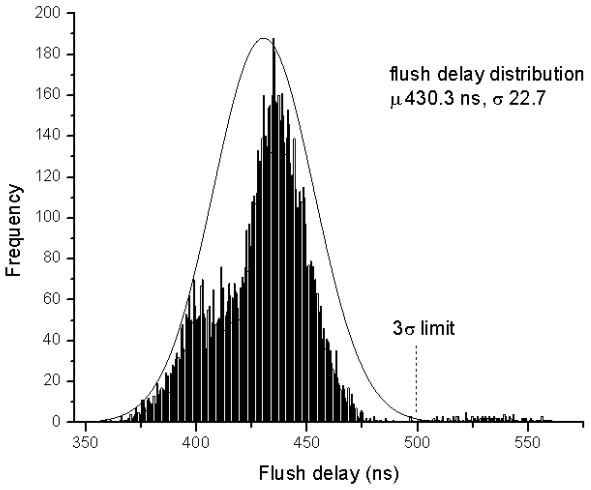


**Fig. 13. Distribution of flush delay for the sample.**

## 6. Experimental Results

We present results from the analysis of the SEMATECH test data. SEMATECH data used a 120K-gate 0.8 μm (0.45 μm $L_{eff}$) technology ASIC as a test vehicle. Four types of tests – functional, stuck-at (scan), delay and $I_{DDQ}$ – were performed at wafer level. A sample of dice was packaged and all tests were performed again. A sample of packaged parts was subjected to various levels of burn-in (BI) and identical tests were performed. $I_{DDQ}$ test used 195 vectors and a pass/fail threshold of 5 μA. This threshold was obtained from the distribution and does not necessarily represent a good manufacturing limit [3]. We limited our data sample to chips that passed all tests or failed only $I_{DDQ}$ and/or delay test at wafer probe. Chips that fail functional or stuck-at test are rejected. In a stop-on-first-fail manufacturing flow, such data may not be available. For each chip we computed CR by taking the ratio of the maximum and the minimum $I_{DDQ}$ values. NCR values were computed by considering all available functional neighbors. The cumulative distributions of CR and NCR values for the data sample are shown in Figs. 14 and 15, respectively. The characteristic long tail of a logarithmic distribution in $I_{DDQ}$ data [14] is observed in the NCR distribution as well. The distribution of chips in the data set according to their wafer and post BI test results is shown in Table 3. They are further categorized based on their CR and NCR values using thresholds obtained from the respective cumulative distributions as shown in Figs. 14 and 15.

***Analysis of CROWNE Chips***

CR outliers with neighbor estimators (CROWNE) show nominal CR but are NCR outliers. These must contain passive or subtle active defects with a high constant defective component of leakage that dominates the

other leakage components. The addition of spatial information is useful for detecting such defects. Such defects can escape the NCR screen only if all neighboring chips have similar or higher defective currents for *all* vectors. Although due to defect clustering there is increased possibility that neighboring chips are defective as well, there is no empirical evidence that all neighboring chips have similar defective currents for all vectors. Since the maximum of all NCR values is used for screening, the NCR screen is more sensitive to defects than CR. Chips with very low CR values (~1) have a strong passive defect. These chips will not cause functional failure at the wafer test, but may fail in the system. There are 138 chips with a CR of 1-1.5 but only one of these chips has a NCR<10. Fig. 16 shows the scatter plot of CR and NCR values for these chips. Detection of passive defects with CR alone may be feasible by setting a lower bound on CR. However, due to the sharp fall of the distribution such threshold setting is difficult [22]. As Fig. 15 shows, setting such a threshold is relatively easy for NCR.

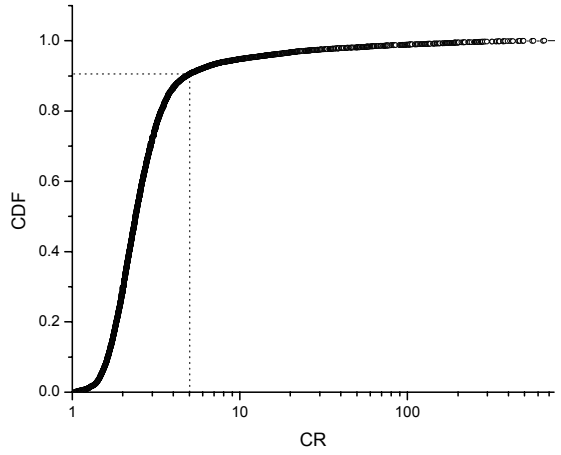


**Fig. 14. Cumulative distribution of CR values.**

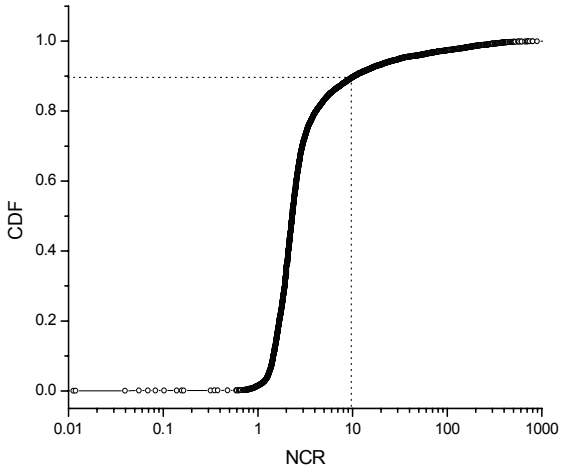


**Fig. 15. Cumulative distribution of NCR values.**

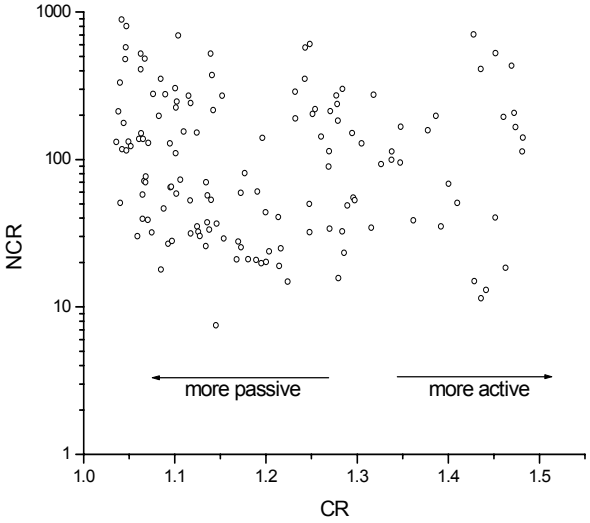


**Fig. 16. CR/NCR scatter plot for low CR chips.**

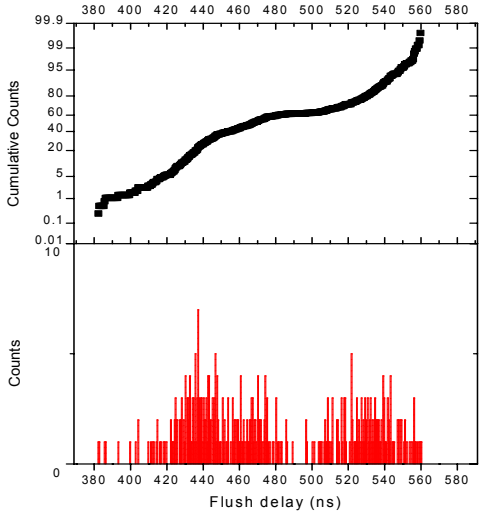


**Fig. 17. Delay failed chips flush delay distribution.**

A total of 336 chips fail only delay tests and 43 chips fail both delay and $I_{DDQ}$ tests. Fig. 17 shows the CDF and distribution of flush delays for these chips and Fig. 18 shows the scatter plot of CR and NCR values. Some of these chips are NCR outliers although they did not fail $I_{DDQ}$ test. Apparently, these delay failures do not seem to be the result of wafer processing conditions. Delay-only failed chips are likely to be due to resistive open defects that do not lead to increase in $I_{DDQ}$. However, a few delay-only failed chips do exhibit high CR and NCR values. The poor correlation between NCR and flush delay (Fig. 19) indicates that NCR alone cannot

be used to screen all chips. For chips from a fast or leaky wafer region, NCR do not change. This can be used to screen defective chips from slow wafer region. However, more data needs to be analyzed to understand relation between NCR and delay-failed chips.

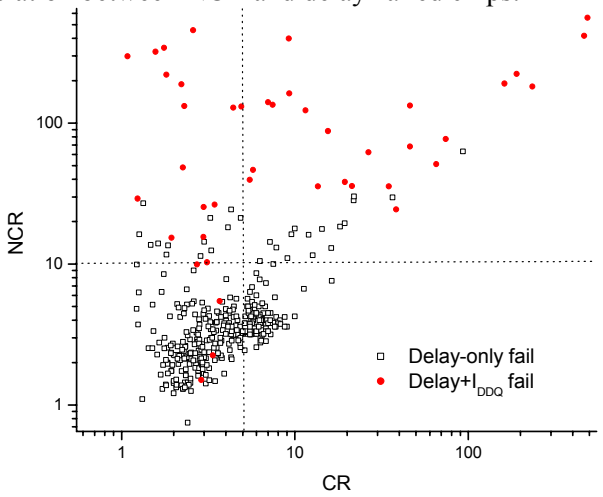


**Fig. 18. CR/NCR scatter plot for chips that fail delay and $I_{DDQ}$ tests.**

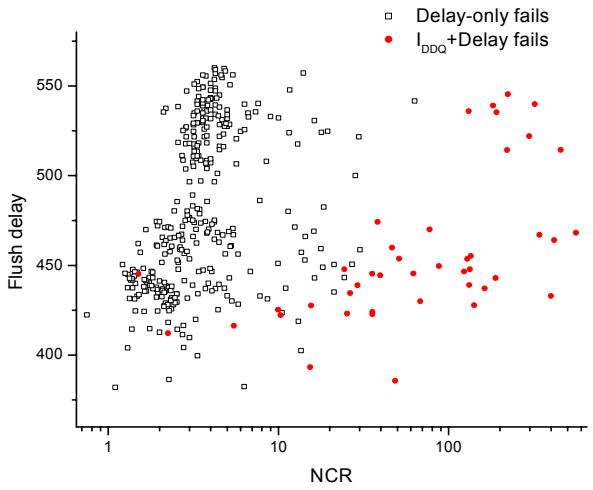


**Fig. 19. NCR/flush delay scatter plot for chips that fail delay and $I_{DDQ}$ tests showing poor correlation.**

## 7. Conclusion and Future Work

We showed that small CR does not necessarily imply fault-free chips as CR falls for passive defects. NCR gleans valuable information and can spot certain outliers. The sensitivity of the CR method to detect outliers is constrained by the number of $I_{DDQ}$ readings. CR/NCR computation and statistical post-processing can be performed on an inexpensive workstation. This computation can be performed before packaging to reduce packaging costs by screening outliers before packaging. The addition of multiple parameters can reveal whether outliers are the result of "normal" process variation or are due to a defect. The correlation between $I_{DDQ}$ readings due to underlying process variations can be exploited by considering each vector as a dimension and representing each chip in a multi-dimensional space [15] and use multi-variable outlier rejection methods.


## Acknowledgements

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