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I_{DDQ} data analysis using neighbor current ratios

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Abstract

I_{DDQ} test loses its effectiveness for deep sub-micron chips since it cannot distinguish between faulty and fault-free currents. The concept of current ratios, in which the ratio of maximum to minimum I_{DDQ} is used to screen faulty chips, has been previously proposed. However, it is incapable of screening some defects. The neighboring chips on a wafer have similar fault-free properties and are correlated. In this paper, the use of spatial correlation in combination with current ratios is investigated. By differentiating chips based on their non-conformance to local I_{DDQ} variation, outliers are identified. The analysis of SEMATECH test data is presented.

Keywords: I_{DDQ} testing; Current ratios; Spatial correlation

1. Introduction

I_{DDQ} testing is a proven test method for screening defective chips. However, it loses its effectiveness as leakage current increases exponentially with shrinking transistor geometries and is considered a difficult challenge [1]. Not only fault-free current is increasing but also variation in fault-free current is rising, thus making distinction between fault-free and faulty currents difficult [2]. Several solutions have been reported in the literature to solve this problem. One possibility is to reduce the background leakage current by using reverse body bias [3] or multiple threshold transistor design. Another method is to exploit the dependence of I_{DDQ} on other parameters like temperature [4,5]. Several solutions reduce fault-free I_{DDQ} variation by statistical means [6,7] or graphical display of data [8] while others use correlation between I_{DDQ} and other parameters [9–11] to make faulty I_{DDQ} values distinguishable. The current ratios (CR) approach has shown some promising results [7]. However, it is not capable of screening certain defects. One solution is to consider additional test information. In this work, we evaluate the capabilities of a combination of the current ratios technique and wafer-level spatial correlation to overcome limitations of CR approach.

In the next section, we review the CR concept and describe the motivation behind this study. Section 3 describes neighbor current ratio (NCR) method. Section 4 describes the results for test data. Section 5 presents discussion and Section 6 concludes the paper.

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2. Current ratios concept

A fault-free chip that leaks more should consume high current for *all* input patterns. On the other hand, a chip having an active (pattern-dependent) defect consumes high current only when the defect is excited. In this case the leakage current depends on the nature and resistance of the defect, among other parameters. Maxwell et al. observed that in spite of an order of magnitude difference in I_{DDQ} values, dice had similar signatures, as shown in Fig. 1 [7]. It was proposed that ratios of maximum I_{DDQ} to minimum I_{DDQ} for fault-free chips would have small variation and can be used as a pass/fail criterion. The signature was described using an equation: Max-I_{DDQ} = Slope · Min-I_{DDQ} + Intercept. Thus, the maximum I_{DDQ} was predicted based on the minimum I_{DDQ} value. The authors characterized a sample of chips and determined current ratios for fault-free chips. Through linear regression they determined the parameters (the slope and the intercept) of the equation shown above. To account for unmodeled process variations, a guard band was added. In production, I_{DDQ} was measured for the minimum I_{DDQ} vector and the pass/fail limit on the maximum I_{DDQ} for all other vectors was set.

Fig. 2 shows the current ratios for SEMATECH chips that passed all wafer tests (11 263 chips) and that failed the 5 μA I_{DDQ} test (1689 chips) [12]. The majority of all-pass chips have small ratios (<3). Some I_{DDQ}-only failed chips (788) have current ratios less than 10, comparable to those of the all-pass chips. Many of these chips either pass all tests or fail only I_{DDQ} test after burn-in (BI). Clearly not all of these chips are so flawed as to be rejected. This indicates that the SEMATECH I_{DDQ} test limit of 5 μA resulted in considerable yield loss.

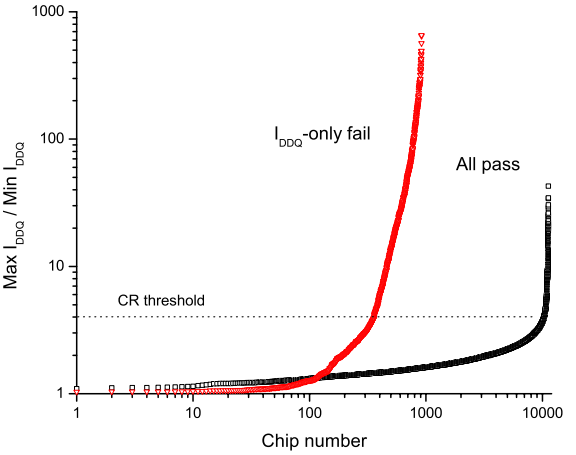

Fig. 2. Current ratios for SEMATECH chips.

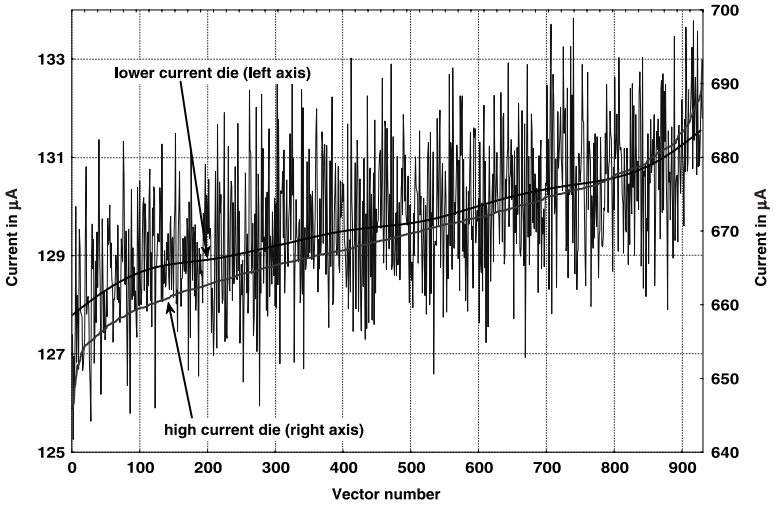

Fig. 1. Current signatures of two dice [7].

3. Neighbor current ratios (NCR)

The total leakage current contains two components: an intrinsic leakage component and a defective leakage component. The minimum I_{DDQ} is mostly due to intrinsic leakage (assuming that at least one vector does not excite the defect or the chip is fault-free). As neighboring chips on a wafer undergo similar processing, their fault-free device parameters are correlated [10]. Therefore, neighboring fault-free chips are expected to have similar current variations. To verify this assumption, we obtained current ratios of all-pass and I_{DDQ}-only failed dice on a wafer. A surface plot with the projection of its contour is shown in Fig. 3. Gross outlier chips having leakage more than 100 μA are not shown. It can be observed from Fig. 3 that except for some outlier chips, CRs vary smoothly across the wafer. The *outlier* chips are likely to be defective and are at a greater risk of failing during BI.

If we obtain ratios of I_{DDQ} readings of a fault-free die and its neighboring dice for each vector, they should exhibit a small variation. We denote these ratios as *neighbor current ratios* (NCR). Let $I_1, I_2, \ldots, I_n$ denote I_{DDQ} readings for a fault-free die (die A) and $I'_1, I'_2, \ldots, I'_n$ denote I_{DDQ} readings for a fault-free neighboring die (die B). Under ideal conditions (no process variations) we obtain:

$$\mathrm{NCR} = \frac{I_1}{I'_1} = \frac{I_2}{I'_2} = \ldots = \frac{I_n}{I'_n} = 1$$

Due to process variations NCRs exhibit small variation around the mean value of unity. If both the chips are fault-free, but one leaks more than the other (passive defect), all NCRs would be consistently more or less than unity. In this case, the mean value would be different but the variance would be small. If both chips contain an active or passive defect, NCR is dependent on the nature of defect and defect current. Fig. 4 shows the histograms of NCRs for five different cases. In each case, a total of 195 NCRs were obtained.

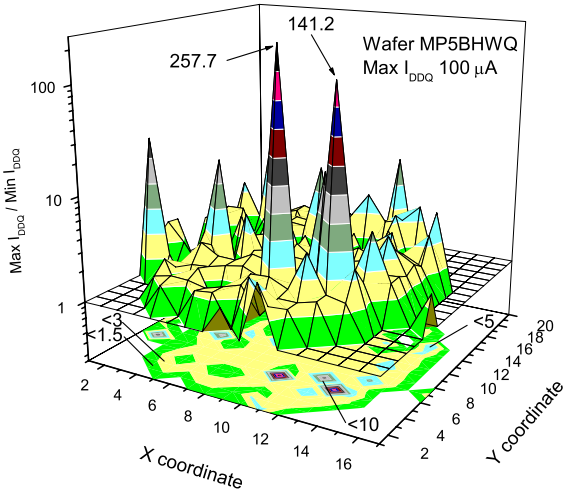

Fig. 3. Current ratio surface and contour plot. For colour see online version.

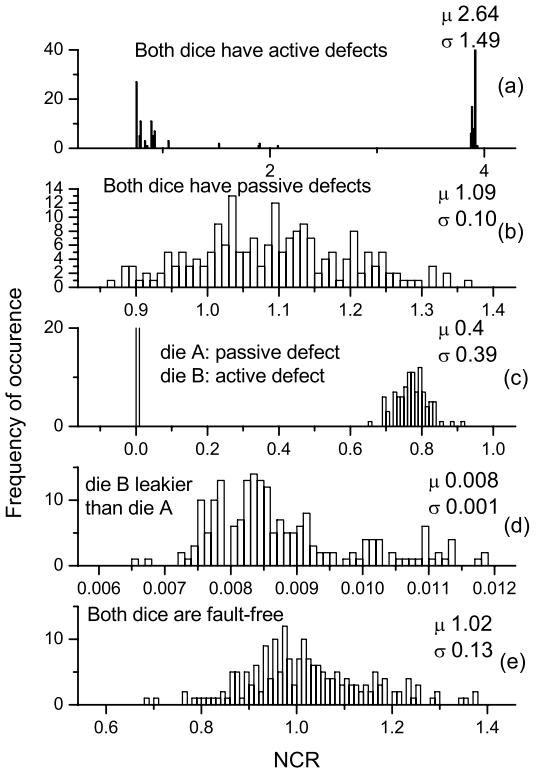

Fig. 4. Histograms of NCRs for different cases.

4. Analysis methodology

The analysis is performed using SEMATECH data [12]. We consider eight neighboring dice for each die. Neighboring chips that fail other than I_{DDQ} test are not considered. Also, chips with very high I_{DDQ} (>100 μA) are not considered in the analysis since such chips are definitely defective. NCRs are computed for all 195 vectors by considering the center die and each neighboring dice. For each die, we obtain the maximum NCR for each available neighbor. The maximum of all NCR values is used for the pass/fail criterion. The NCR value essentially indicates the *degree of conformity* of a chip to its neighbors. Thus, a chip having very high NCR is more likely to contain a defect and fail than a chip having NCR close to 1. NCR-based rejection is expected to reduce the yield loss by rejecting only gross spatial outliers.

Fig. 5 shows the NCR wafer surface plot for the same wafer shown in Fig. 3. Notice that several chips having small current ratios in Fig. 3 (likely passive defects) exhibit much higher maximum NCR in Fig. 5. Thus use of NCR can improve the confidence in outlier detection. Fig. 6 shows maximum NCRs for all chips that passed all wafer level tests or failed only I_{DDQ} test. All pass chips show a long tail (outlier chips) indicating not all

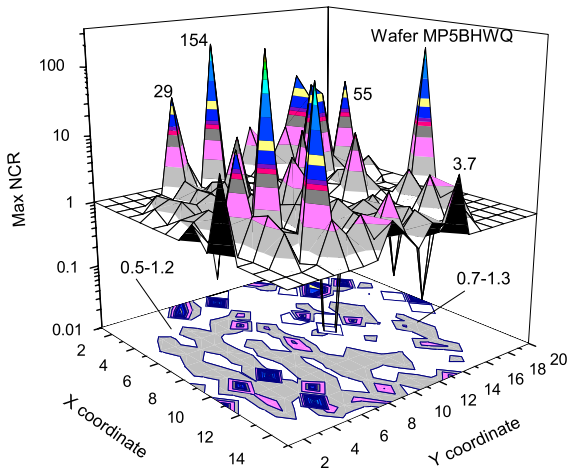

Fig. 5. NCR surface and contour plot. For colour see online version.

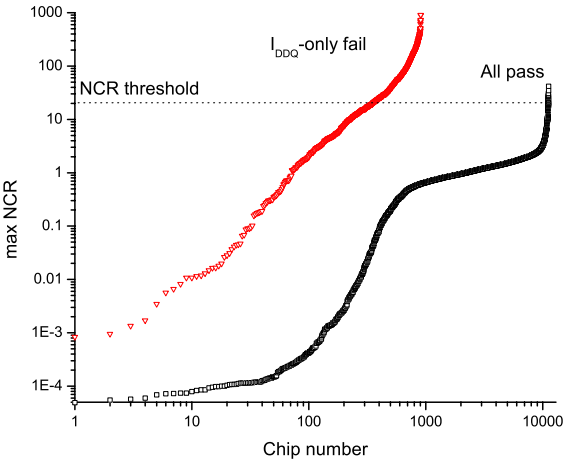

Fig. 6. NCRs for SEMATECH chips.

chips are fault-free. On the other hand, many I_{DDQ}-only failed chips have NCR values (<10) comparable to that of all pass chips.

It is difficult, if not impossible, to distinguish NCRs of two fault-free chips and two chips with passive defects. However, it is unlikely that all the neighbors have identical passive defects with similar currents.

5. Experimental results

To evaluate the effectiveness of NCR, we used SEMATECH data. We considered only those chips that passed all tests (1102) or failed only I_{DDQ} test (1558) at the wafer level and underwent 6 hours of BI. All chips for which I_{DDQ} exceeded 100 μA were considered to have a gross defect and were ignored from the analysis. This reduced the dataset from 1558 I_{DDQ}-only fails to 858 I_{DDQ}-only failed chips. Since we considered only immediate neighboring die positions, 19 dice having zero adjacent neighbors could not be considered for analysis. The total dice in the dataset were 1941 (1098 all pass, 843 I_{DDQ} fail). For each available neighbor a total of 195 NCRs were obtained and the maximum NCR was used for pass/fail decision.

To compare the effectiveness of NCR with current ratios, we considered the same dataset and used current ratios for the pass/fail decision. We

used a current ratio of 4 (from Fig. 2). The NCR threshold was adjusted (21) to obtain the same defect level obtained by the CR method. While computing the defect level, all post-BI I_{DDQ}-only failed chips were considered fault-free.

Table 1 shows the distribution of chips in different categories. All chips are divided into two main categories: chips accepted by current ratio (CR accept) and chips rejected by current ratio (CR reject). They are further subdivided into two categories: chips accepted by neighbor current ratio (NCR accept) and those rejected by neighbor current ratio (NCR reject). These four categories are divided depending on their wafer probe result: (a) chips that passed all SEMATECH tests (''All pass'') and (b) chips that failed the 5 μA threshold I_{DDQ} test but passed other tests (''I_{DDQ}-only fail''). Each category is subdivided based on post-BI SEMATECH test result. This distinction is made to understand the distribution of NCRs and CRs in different categories and understand if certain chips get detected by one method but not by the other and rejection rate of healer chips. Since the 5 μA test limit does not represent a ''good'' manufacturing limit [12], the difference in I_{DDQ}-only failed chips detected by one method but not the other would be statistically significant to draw meaningful conclusions.

The overkill and defect level are computed by dividing the number of chips that pass (fail) after BI by the total number of chips rejected (accepted) as a percentage. These values are scaled appropriately considering the entire population that was not burned in. Table 2 shows overkill and defect level (DL) values for both methods and their combination. In the combined method a chip is rejected if it is considered faulty by either method. Since I_{DDQ}-only fail chips are not conclusively defective, overkill and DL are computed by considering all such chips fault-free and then by considering all such chips faulty. This is indicated in the second row. The columns headed ''Good'' (''Faulty'') have overkill or defect levels values computed by considering all I_{DDQ}-only failed chips fault-free (faulty). The actual values would lie between these two extremes. The effective yield is the percentage of total chips (1941) accepted by a method.

Table 1
Distribution of chips for different test methods

SEMATECH wafer probe test result	CR Accept		CR reject		Post-BI SEMATECH test result
	NCR accept (1153)	NCR reject (149)	NCR accept (280)	NCR reject (359)	
All pass	949	0	100	3	All pass
	19	0	7	1	I_{DDQ} fail
	17	0	2	0	Other
I_{DDQ}-fail	69	26	76	54	All pass
	94	119	90	295	I_{DDQ} fail
	5	4	5	6	Other

Table 2
Overkill and DL for different test methods

Metric	Overkill %		Defect level %		Effective yield %
I_{DDQ} fail	Good	Faulty	Good	Faulty	
CR	97.97	36.46	2.00	19.82	67.08
NCR	98.03	16.34	2.02	16.68	77.83
CR + NCR	97.84	32.87	1.91	11.71	59.40

6. Discussion

Table 1 reveals many interesting findings. Since both NCR and CR thresholds are high, only 3 of the all pass chips at wafer probe are rejected by both methods. The NCR test rejects fewer chips that pass all wafer tests than the CR test. The SEMATECH data has many healer chips that have reduced I_{DDQ} after BI (and thus pass all tests). Since NCR threshold is very loose it accepts more healer chips than CR test. Since healers represent unstable or unreliable chips, they are rejected up front in a test flow. In practice, NCR threshold should be selected by observing wafer-level variation in I_{DDQ}. NCR test rejects more chips that fail wafer level and post-BI I_{DDQ} test than the CR test. Considering the NCR threshold is 21, these chips are more likely to be defective.

Fig. 7 shows the distribution of post-BI failures of chips according to their maximum NCR. The healer chips are shown separately. As expected, the bins with maximum NCR values less than 2.5 have a high percentage of fault-free chips. As expected the bins for high NCR values have higher failure rates. Since the BI sample was non-uniform, some higher NCR bins have very few chips resulting in low failure rates. But for all practical purposes, it is safe to assume that NCR values higher than 10 would have high failure rate. The bins with NCR values much less than 1 represent good dice in bad neighborhood (*spatial dips*). Previous work has shown that the probability of failure of such dice is high [13]. Several chips having maximum mean NCR less than 1 pass all post-BI tests. Some of these chips are more likely to contain subtle defects and fail sooner.

The bins with NCR values greater than 10 essentially represent bad dice in good neighborhoods (*spatial peaks*). Such spatial outliers can be easily identified by the NCR test method. As Fig. 7 indicates the probability that such chips will pass BI falls with higher NCR values. Many of these chips are healers and hence unreliable.

NCR test rejects more I_{DDQ}-only failed chips than the CR test. This gives a yield penalty for a fast wafer region. Another metric like flush delay can be combined with NCR values to reduce the yield loss [14]. Even if a single die in the neighborhood yields high NCR for the center die, the center die should be regarded as defective and rejected or subjected to BI.

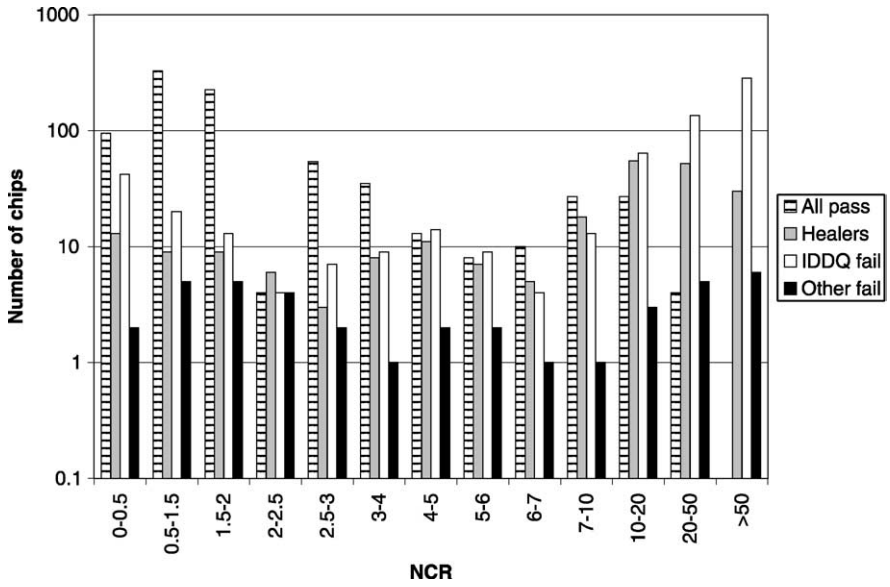

Fig. 7. Distribution of post-BI results of chips for different maximum NCR values.

6.1. Advantages of NCR

NCR is an intuitively simple metric. It can be used to screen high leakage current chips surrounded by good chips as well as detect good chips in a bad neighborhood (*spatial dips*). Only a single good neighboring die is necessary for NCR test. This is generally not a problem except in a poor yield zone or on the wafer edge. Since NCR is self-calibrating and self-scaling it provides an easy way to use spatial information for I_{DDQ} pass/fail decisions for any technology node.

6.2. Limitations of NCR

The basic assumption of NCR is that neighboring chips have I_{DDQ} values that are correlated. If the neighboring chips are missing, the NCRs cannot be determined. This is true for dice on the wafer edge and in a poor yield zone. It can be resolved by considering dice at longer distances [9]. To account for lot and wafer level variations, it is helpful to find the best predictors for each die position. Dice on the wafer edge could be correlated to dice on the edge either on the same wafer or on another wafer [15].

7. Conclusions and future work

It is shown that comparing the I_{DDQ} of a die with that of its neighboring chips and observing the variation can be useful for spotting local spatial outliers. For the same defect level, the NCR-based test has a higher yield and lower overkill compared to current ratios. This test method assumes that wafer level variation in fault-free parameters is smooth, which is usually the case. If stepper field patterns exist in the wafer test data, it is necessary to identify the best predictors for each die position similar to the study reported in [16]. It would be interesting to see if combination with other parameters or other test methods such as delta-I_{DDQ} improves the results. It will be interesting to do vector and neighbor sensitivity analysis of NCR and compare its performance with CR.

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