NCR: A Self-scaling, Self-calibrated Metric for I_{DDQ} Outlier Identification

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Abstract

I_{DDQ} testing is an important component of a test suite. However, increasing leakage current values with each technology node render single pass/fail limit setting approach obsolete. This is further worsened due to increasing process variations and discriminating faulty and fault-free chips is becoming increasingly difficult. In this paper we evaluate a metric that uses wafer-level spatial information to identify faulty dice on a wafer. The metric is evaluated using industrial test data[§].

1. Introduction

The traditional leakage current (I_{DDQ}) test method uses a single pass/fail limit for accepting or rejecting chips. In this method I_{DDQ} is measured for a number of input vectors. If it exceeds the predetermined limit (pass/fail threshold) the chip is considered defective and rejected. The pass/fail limit can be determined by circuit simulations [1] or empirically. The continuous advances in semiconductor manufacturing technology have resulted in shrinking transistor geometries. As transistor geometries are reduced, the corresponding reduction in threshold voltage for retaining high performance results in an exponential increase in I_{DDQ} [2]. This is exacerbated by increasing process variations with each technology node [3] and is considered to be a tough challenge by International Technology Roadmap for Semiconductors (ITRS) [4]. As shown in Figure 1, since fault-free and faulty leakage current distributions overlap for deep sub-micron (DSM) technologies, single pass/fail limit invariably results in rejection of fault-free chips (yield loss, region A) or acceptance of faulty chips (defect level, region B) [5]. Thus single pass/fail limit setting cannot survive in its present form.

In a recent study it was observed that several chips fail *only* I_{DDQ} test at wafer level and after burn-in [6]. Clearly not all chips are defective. The chips that have markedly different parameters than the rest of the chips from the same wafer or lot are considered *outliers*. Identifying outliers early in the production cycle is important to reduce test costs. Such chips can be rejected earlier in a test cycle or selectively burned in, thus reducing overall test time or yield loss. Outlier identification can be useful in providing valuable feedback to the foundry to understand process glitches as well. The behavior of some of the seemingly outlier chips can be explained by understanding underlying process variations and can be shipped thus reducing the potential yield loss.

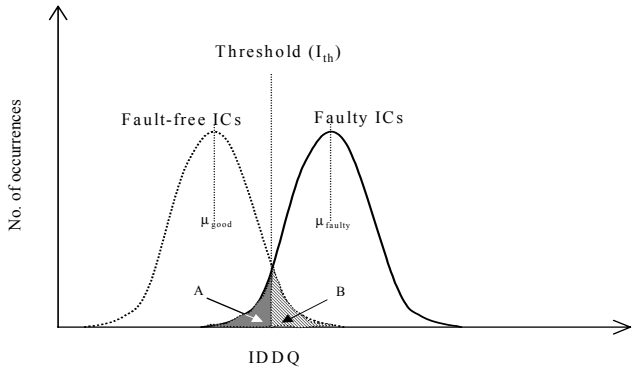

Figure 1: Fault-free and faulty I_{DDQ} distributions overlap for DSM technologies

In this paper we evaluate the use of neighboring chip information for identifying outlier chips at the wafer level. The remainder of the paper is organized as follows. In Section 2 we describe the motivation in using spatial wafer level information. Section 3 defines the metric and the analysis methodology. Section 4 includes the experimental results and finally Section 5 concludes the paper.

2. Motivation

Several methods have been proposed in the literature for I_{DDQ} testing [7, 8, 9, 10]. In particular, the current ratios technique [10] has shown some promising results. The basic idea behind current ratios is that in spite large inter-die variation in I_{DDQ}, the ratios of the maximum to the minimum I_{DDQ} (called *current ratio*) for fault-free dice are similar. Thus a chip having a different current ratio is likely to be defective. This method was implemented in production at Agilent Technologies. The authors

[§] This data comes from the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The conclusions drawn are our own and do not necessarily represent views of International SEMATECH or its member companies.

characterized a sample of chips and determined the range of (fault-free) current ratios through linear regression [10]. The vector that yielded minimum I_{DDQ} for a majority of chips was identified. In production, after measuring I_{DDQ} for the minimum I_{DDQ} vector, the limit on all other vectors was set so as not to exceed the current ratio. Unfortunately, the minimum I_{DDQ} vector is not same for all chips. Thus the current ratio would accept some defective chips. On the other hand, it can result in rejecting some fast but leaky chips.

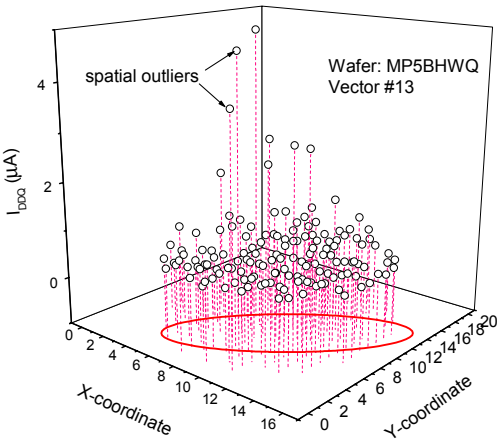

Figure 2: Wafer-level spatial variation in I_{DDQ}

Since neighboring dice on a wafer are subjected to similar manufacturing conditions, their fault-free parameters are correlated. Thus neighboring chips on a wafer are expected to have *similar* I_{DDQ} values. This fact can be exploited to identify true outlier (defective) chips. Figure 2 shows a wafer level variation in I_{DDQ} for a vector. It can be observed that a majority of chips have similar I_{DDQ} and exhibit smooth wafer level variation. Some defective chips having leakage currents much higher than their immediate neighbors are clearly distinguishable. These are termed as *spatial outliers*. The chips that exhibit nonconformance to local wafer region contain some latent defect and are likely to fail early in the system. Thus it is important to screen them from reliability point of view.

N1	N2	N3
N4		N5
N6	N7	N8

Figure 3: Immediate neighborhood definition

3. NCR Metric Definition

For the same vector, two chips are expected to have similar I_{DDQ}. Neighbor Current Ratio (NCR) is obtained by taking ratio of I_{DDQ} of a chip and that of its neighbor for the same vector. Thus ideally (for fault-free chips under no process variations) NCR is equal to 1. However, owing to process variations NCR values would vary.

Mathematically, NCR is defined as follows:

$$NCR_{ji} = \{\frac{I_{ci}}{I_{ji}}\} \quad \forall i \, and \, 1 \le j \le 8$$

where I_{ci} is I_{DDQ} of the center die for the i^{th} vector and I_{ji} is I_{DDQ} of the j^{th} neighboring die for the i^{th} vector.

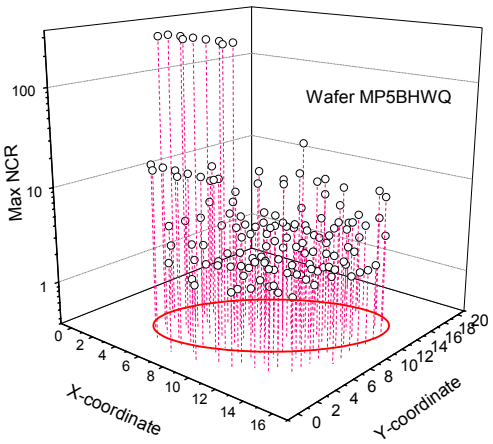

Figure 4: NCR variation across wafer

Analysis Methodology

The analysis is done at the wafer level. For each die on a wafer we consider immediate neighboring dice as shown in Figure 3. The die under test is shaded (at the center) and the neighboring dice are marked as N1 through N8. Any die that fails functional, stuck-at or delay test is ignored from the analysis. In production, I_{DDQ} data is usually not available for such hard fails. Also dice having gross defect and very high leakage current are not considered. Such chips have some gross defect and are rejected even if they pass all other tests due to reliability risk. The dice on the wafer edge and in poor yield zone have fewer neighbors. Dice that have no immediate neighbors are ignored from the analysis. Figure 4 shows the variation in maximum NCR values across the wafer shown in Figure 3. Notice that many spatial outliers are now visible. The fault-free dice form a cluster (0.5<NCR<2.5) near the center of the wafer while some dice are obvious outliers (NCR>100).

Pass/Fail Criterion

The goal of NCR is to find outliers by comparing I_{DDQ} variation of the neighboring dice. Since our goal is to find out *maximum* nonconformance to the local neighborhood chips, the maximum NCR (*maxNCR*) value is used for pass/fail criterion. The mean (μ) and standard deviation (σ) of NCRs is obtained by computing NCRs for all vectors, for all neighboring chips. If *maxNCR* exceeds the mean+3σ limit, the chip is considered defective and rejected.

4. Experimental Results

We used the SEMATECH test data to evaluate NCR metric. In the SEMATECH experiment four types of test – functional, stuck-at, delay and I_{DDQ} – were performed on a total of 18466 chips. The I_{DDQ} test used the pass/fail threshold of 5 μA. A total of 195 I_{DDQ} readings were collected for each chip. If any I_{DDQ} reading exceeded 5 μA, the chip was considered I_{DDQ} fail. A sample of chips was subjected to six hours of burn-in and a smaller sample was subjected to 72 hours of burn-in (extended burn-in).

We considered only chips that passed all tests or failed only I_{DDQ} test at the wafer level and underwent 6 hours of burn-in. We also rejected chips having I_{DDQ} more than 100 μA for any vector. This limit is 20 times SEMATECH pass/fail threshold and is very loose. Such chips have gross defects. The total number of chips in the data set were 1940 (1098 all pass and 842 I_{DDQ}-only fail). For each chip, NCRs were computed for each neighbor for all 195 vectors. It the *maxNCR* of a chip exceeded the 3-sigma limit it was rejected. Due to I_{DDQ} variation across wafer, this resulted in different limits for each chip. This also accounts for local process variations.

Table 1 shows the distribution of chips in various categories. The first column shows the wafer probe result. The chips are divided in two categories: those accepted by NCR metric and those rejected by NCR metric. They are further subdivided depending on their six hours post burn-in (BI) test result.

Table 1 reveals many interesting findings. Many chips fail only I_{DDQ} test before BI and pass all tests after burn-in. This healing of a defect can result due to evaporation of the metal/poly sliver during BI. The healers are essentially unstable or unreliable chips and are not shipped. The 3-sigma limit seems to be too optimistic for such chips.

There are several chips that fail only 5 μA I_{DDQ} test before and after burn-in. NCR accepts a large number of these chips indicating that their I_{DDQ} variation conforms to the local neighborhood I_{DDQ} variation. It has been observed that defects tend to cluster on a wafer due to a phenomenon called *defect clustering* [11]. This can potentially mislead NCR analysis and result in accepting defective chips. Such chips would eventually fail in system. However, since we used all 195 NCR values, the probability of accepting defective dice is extremely small.

To verify that the most of the dice accepted by NCR are indeed fault-free, we considered the sample subjected to extended hours of burn-in. A total of 465 chips accepted by NCR were burned-in for 72 hours. Table 2 shows the distribution of these chips in various categories. A large number of chips consistently pass all tests at all levels. A majority of chips consistently fail 5 μA I_{DDQ} test. Since this pass/fail limit does not represent a good manufacturing limit [6], these chips are not necessarily defective. Owing to the fact that burn-in sample was biased toward I_{DDQ} fails [6] and only 10 out of 340 chips fail a voltage test after extended burn-in supports this claim.

Table 1: Distribution of chips

Wafer Probe	NCR Accept	NCR Reject	Post Burn-in
All pass	849	203	All pass
	18	9	I_{DDQ} fail
	12	7	Other fail
I_{DDQ} fail	134	91	All pass
	428	170	I_{DDQ} fail
	14	6	Other fail

Table 2: Distribution of chips accepted by NCR according to their post-extended burn-in test results

Wafer Probe	Six hours burn-in result			Extended Burn-in Result
	All pass	I_{DDQ} fail	Other	
All pass	110	0	0	All pass
	2	6	0	I_{DDQ} fail
	5	0	0	Other fail
I_{DDQ} fail	0	7	0	All pass
	0	323	2	I_{DDQ} fail
	0	10	0	Other fail

Figure 5 shows the distribution of the post burn-in results of chips for various NCR values. It can be observed that chips with NCR values more than 10 have much higher failure rate. Thus spatial outliers detected by NCR are likely to fail burn-in. Several spatial outliers also exhibit healing behavior after burn-in. Since these represent unreliable chips, NCR can be used to screen them at the wafer sort.

Defect Level and Yield Loss Calculations

The defect level (DL) and yield loss (YL) are calculated as follows.

$$DL = \frac{Number\ of\ accepted\ chips\ that\ fail\ any\ voltage\ test\ after\ BI}{Total\ number\ of\ chips\ accepted\ by\ NCR}$$

$$YL = \frac{Number\ of\ rejected\ chips\ that\ pass\ all\ tests\ after\ BI}{Total\ number\ of\ chips\ rejected\ by\ NCR}$$

The healers are not counted while computing YL. From Table 1 data the DL and YL values are 1.78% and 41.77%, respectively.

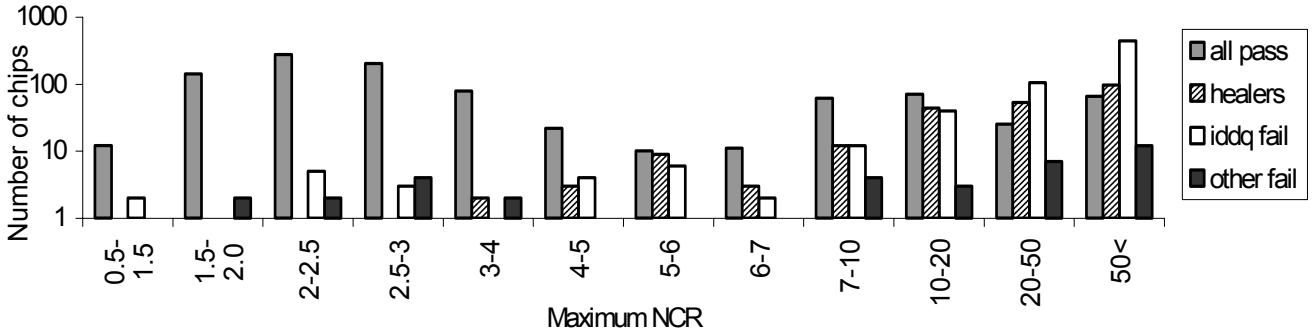

Figure 5: Distribution of post burn-in results for different NCR values

The yield loss value appears to be very aggressive because of the pessimistic limits set in the good wafer region. In the fault-free region of a wafer, because of similar I_{DDQ} values, the standard deviation is very small. Thus a slight deviation from the mean value can result in rejection of the chip. Since we use maximum NCR for pass/fail limit, such chips are pessimistically rejected. Alternatively, the use of mean NCR value instead of maximum NCR can result in lower yield loss.

5. Conclusions

As outlier identification becomes increasingly difficult, alternative methods must be sought. In this work, we presented a metric that uses wafer level spatial information for identifying defective leaky devices. NCR is intuitively simple and straightforward metric that is independent of technology scaling. The nominal value is automatically fixed to unity according to definition.

The limit setting issue still remains. It is always a trade off between quality (defect level) and cost (yield loss). However, identifying chips having high reliability risk early in the production can result in test cost reduction. Such chips could be screened or selectively burned-in. More importantly, NCR can be helpful in understanding "bad zones" on a wafer or to monitor process glitches.

Some chips could be leaky and fast (due to reduced effective channel length). NCR cannot distinguish between fast chips on the edge of fast wafer zone and defective chips. This distinction can be achieved by correlating multiple parameters like flush delay along with NCR [12]. The limits could be set as a function of gradient in NCR across wafer. When no immediate neighboring dice are available, dice at longer distances can be used for NCR computation. The identification of the best predictors for each die position similar to the study reported in [13] can result in reduced yield loss.

Acknowledgements

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