Use of Multiple I_{DDQ} Test Metrics for Outlier Identification

Sagar S. Sabade D. M. H. Walker
Department of Computer Science
Texas A&M University
College Station, TX 77843-3112
Tel: (979) 862-4387
Fax: (979) 847-8578
E-mail: {sagars, walker}@cs.tamu.edu

Abstract

With increasing circuit complexity and reliability requirements, screening outlier chips is an increasingly important test challenge. This is especially true for I_{DDQ} test due to increased spread in the distribution. In this paper, the concept of current ratio is extended to exploit wafer-level spatial correlation. Two metrics – current ratio and neighbor current ratio – are combined to screen outliers at the wafer level. We demonstrate that a single metric alone cannot screen all outliers, however, their combination can be used for effectively screening outlier chips. Analyses based on industrial test data are presented.

Keywords: Current ratio, neighbor current ratio, spatial correlation, outlier identification, I_{DDQ} testing

1. Introduction

Leakage current or I_{DDQ} test faces difficult challenges in the deep sub-micron (DSM) era [1]. This is primarily due to the increase in the magnitude and the variation in fault-free I_{DDQ}, which makes distinction between faulty and fault-free chips difficult [2][3]. The traditional single threshold test method therefore becomes obsolete. Several solutions have been proposed in the literature to solve this problem [4][5][6][7][8][9][10][11][12][13]. In particular, the Current Ratio (CR) technique proposed by Maxwell et al. [7] was shown to have better screening capability than the single threshold method. This technique is worth pursuing because it is relatively easy to implement in production and it is claimed to be scalable to future technologies.

In this paper, we review the underlying assumptions of the CR method and examine its limitations. To screen defective chips not caught by CR it is necessary to use another metric in conjunction with CR. We propose one such metric, called Neighbor Current Ratio (NCR), that exploits wafer-level spatial correlation, and examine the outlier screening capability of a CR/NCR combination.

The remainder of this paper is structured as follows. In the next section, we describe the assumptions of the CR method and using empirical data show how they can lead to excessive test escapes. In Section 3 we describe the NCR concept and motivation behind using this as a secondary metric. Section 4 illustrates different cases that arise by combining these two metrics. In this section we also discuss why a single metric is insufficient. Some insights obtained by the CR/NCR combination based on industrial burn-in data are described in Section 5. Finally, Section 6 concludes the paper.

2. Current Ratios – Assumptions and Reality

The intra-die intrinsic variance in I_{DDQ} is much smaller than the inter-die intrinsic variance in I_{DDQ} [14]. This is because the intra-die variation mostly results from the circuit topology (which/how many paths are turned on/off) and the inter-die variation stems from process fluctuations across wafer/lot. The variation-induced change in leakage current is uniform for all vectors. Thus a fast chip would leak more on all vectors. Therefore fault-free chips show deterministic vector-to-vector variation in I_{DDQ}. The I_{DDQ} value of each vector will also vary from chip to chip.

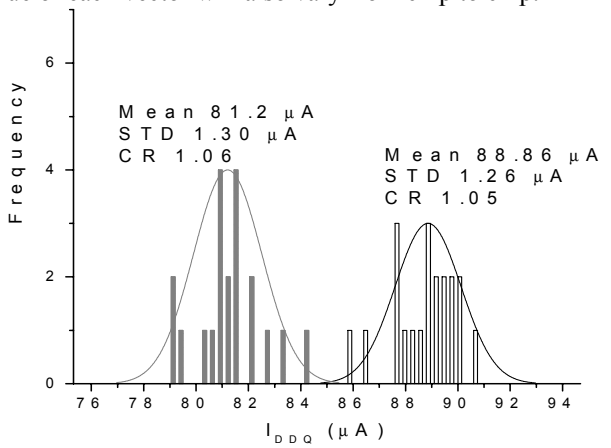

Figure 1. Two chips having different I_{DDQ} values exhibit similar CR due to the underlying process-design interaction.

The concept of CR is based on the assumption that the intra-die variance in I_{DDQ} is small in the absence of a defect. The CR is the ratio of the maximum I_{DDQ} to the minimum I_{DDQ} of a chip. Maxwell et al. observed that in spite of several orders of magnitude variation in fault-free I_{DDQ} itself, the CRs of fault-free chips were similar [7]. They used this fact to measure current for the vector resulting in minimum I_{DDQ} and to set limits on all other vectors so as not to exceed the CR threshold determined through empirical analysis. Figure 1 shows I_{DDQ} distributions of two chips from a wafer. Although the two chips have different I_{DDQ} values, they have similar variance and CR.

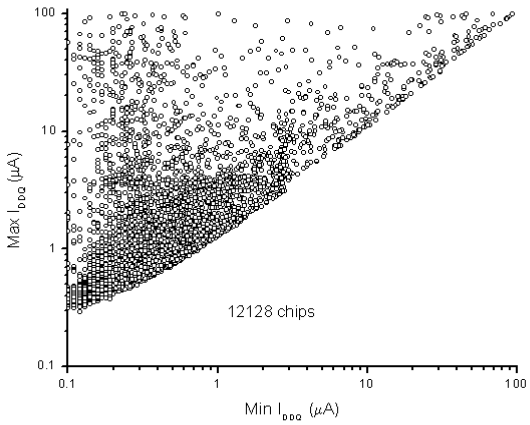

Figure 2. Variation in current ratios for SEMATECH chips that passed all tests or failed only I_{DDQ} test at the wafer level.

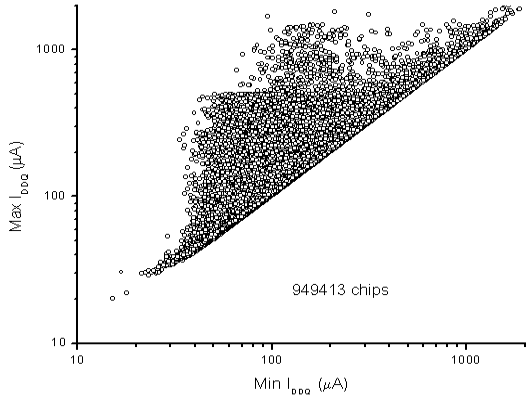

Figure 3. Determining appropriate threshold for current ratio is challenging due to large inter-die variance.

Although the current ratio method holds promise for present and future technologies, determining the appropriate pass/fail threshold for current ratios is not straightforward. Figure 2 shows the variation in the minimum and maximum I_{DDQ} for SEMATECH[1] chips [15] that passed all tests or failed only I_{DDQ} test (5 μA threshold) at the wafer level. Figure 3 illustrates similar spread in the minimum and maximum I_{DDQ} values for a total of 949753 chips from 1342 different wafers across different lots from recent industrial test data. In both graphs, the ratio of ordinate to abscissa (slope) gives the CR. It can be clearly seen that deciding a "fault-free" CR threshold is not easy. Too small a threshold would result in excessive yield loss. Notice that many chips cannot be conclusively termed *outliers*. Hence determining an appropriate CR threshold is difficult. Some of the chips having nominal CR are "spatial outliers" – chips exhibiting much higher current than their immediate neighbors on the wafer. Such chips are likely to fail (reliability risk) even if they pass all Boolean tests [11].

Given several orders of magnitude variation in fault-free I_{DDQ} itself, understanding the bounds of "fault-free" variation is vital for setting an appropriate pass/fail limit. Knowing the maximum permissible spatial variation in fault-free I_{DDQ} at the wafer level can be helpful for this purpose.

3. NCR Concept

Process parameters vary smoothly across a wafer. Therefore neighboring chips on a wafer have similar fault-free parameters. Wafer-level spatial correlation has been shown to be useful in screening defective chips [10][11][16]. Figure 4 shows a wafer surface plot of I_{DDQ} for a single vector. Note that except for a few outliers fault-free leakage currents of neighboring chips on a wafer are similar. Based on this observation we proposed an alternative metric called Neighbor Current Ratio (NCR) [17].

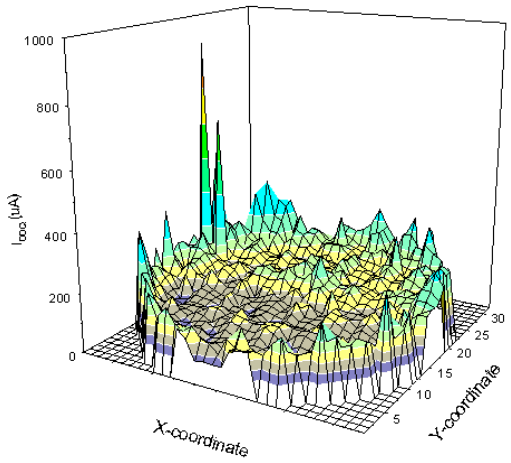

Figure 4. Surface plot of leakage current for a wafer.

The NCR is defined as the ratio of leakage current of a chip to the leakage current of a neighboring chip (eight adjacent chips on the wafer are considered neighbors) for the same vector. NCR can be computed for each vector pair for the center die and all its neighbors. Since neighboring chips have similar fault-free leakage currents for the same vector, the nominal value of NCR is 1. Of course, owing to process variations NCR values for a fault-free chip will vary, generally having a Normal distribution with mean value of 1 (assuming fault-free neighbors). We take the maximum of all NCR values since it is most sensitive to defects, as we are interested in using maximum nonconformance to the local neighborhood for screening outliers. The nominal value of the maximum NCR is more than 1 since at least one vector on a neighbor will have a lower I_{DDQ} value. Table 1 lists different defect possibilities as implicated by NCR values. A passive defect such as a V_{DD}-GND short has elevated I_{DDQ} for all vectors. Active defects produce elevated I_{DDQ} for some but not all vectors.

[1] This data comes from the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The conclusions drawn are our own and do not necessarily represent the views of SEMATECH or its member companies.

When both the chips have passive defects, NCR depends on the relative magnitudes of defect currents for two chips.

Table 1. Various possibilities for NCR (die A I_{DDQ}/die B I_{DDQ}).

Die A	Die B	NCR
Fault-free	Fault-free	~1
Fault-free	Passive Defect	<1
Fault-free	Active Defect	<1
Passive Defect	Fault-free	>1
Active Defect	Fault-free	>1
Active Defect	Passive Defect	Depends on nature of defect
Passive Defect	Active Defect	
Passive Defect	Passive Defect	
Active Defect	Active Defect	

4. Outlier Detection by Combined Metric

The scatter plot of CR and NCR values for SEMATECH chips that passed all tests or failed only I_{DDQ} test at wafer probe is shown in Figure 5. Chips having I_{DDQ} of more than 100 μA are rejected as gross outliers [18] and are not shown. Both CR and NCR values show long tails due to outliers. Considering more than an order of magnitude intra-die variation unlikely for a fault-free chip (since the SEMATECH test chip was I_{DDQ} testable), chips can be divided in four regions as shown in Figure 5. The thresholds can be determined by observing the distributions of CR and NCR. Note that several chips that appear to be inliers with CR alone are outliers when NCR values are considered. CR essentially considers intra-die leakage but comparison with other chips is implicit through the characterization process. It does not consider wafer-level variations at the test application time. Since several orders of magnitude variation is observed across wafers [14] it is necessary to understand whether the increased intra-die leakage (high CR) is due to intra-die process variation and whether it is within the "tolerable" bound for a given wafer region. NCR achieves this by estimating inter-die variation using immediate neighboring chips to reveal nonconformance to the local neighborhood. If every vector activates a defect to some degree, intra-die variance in I_{DDQ} can remain relatively low. In this case, the chip can have nominal CR but is likely to have high NCR.

Another CR/NCR scatter plot using industrial test data is shown in Figure 6. The distribution of CR and NCR values is shown in Figures 7 and 8, respectively. CR depends on minimum and maximum I_{DDQ} current of a chip. The minimum I_{DDQ} stems from intrinsic leakage and is expected to have lognormal distribution [11]. The maximum I_{DDQ} is dependent on the nature of a defect and therefore does not fit any standard distribution. As a result, the CR distribution cannot be described by any standard distribution. In general, both CR and NCR distributions for chips from different wafers/lots have a long tail due to outliers. The thresholds are normally set so as to limit the number of chips accepted from the tail of the distribution and are always a trade off between quality and overkill. Due to the rapid changes in CR frequency near 1 and the long tail, the normality assumption of Chauvenet's criterion [19], the Tukey method [20] or similar outlier rejection methods can result in tremendous overkill. For Figure 6 the conventional $\mu+3\sigma$ thresholds would be 1.83 for CR and 6.43 for NCR. The skew and long tail of the distributions make it difficult to find normalizing transforms. A threshold of 1.8 for CR would reject 8643 (<1%) chips. A threshold of 6.5 for NCR would reject 1777 (0.1%) chips. We chose a slightly looser threshold for NCR than CR based on the assumption that CR will catch most defective chips, and the NCR threshold primarily targets more subtle defects. For a total of 736 chips, both CR and NCR values are above the respective thresholds.

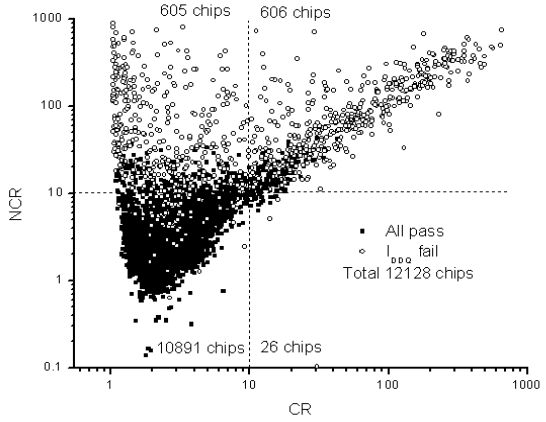

Figure 5. CR/NCR scatter plot for SEMATECH chips that passed all tests or failed only I_{DDQ} test (I_{DDQ} < 100 uA). The number of chips in each region are shown.

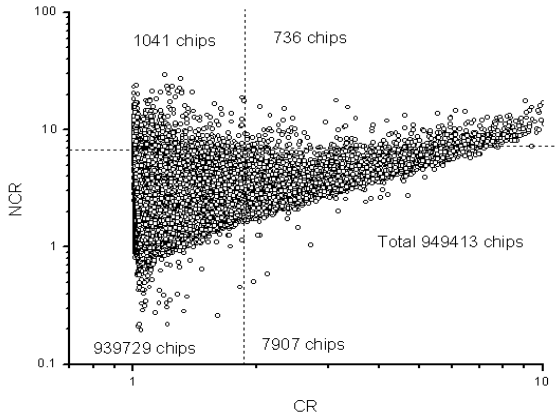

Figure 6. CR/NCR scatter plot for recent industrial data showing number of chips in each region.

It is relatively easy to reject chips with a strong active defect, as their CRs are high. Such chips also have high NCRs since high NCR requires only a single neighbor with one fault-free I_{DDQ} reading. Notice that in Figures 5 and 6 NCR is mostly in agreement with CR for chips having elevated leakage due to active defect in the upper right region.

The presence of a passive defect lowers the current ratio or does not change it appreciably depending on the relative magnitudes of background leakage and defect currents. As the relative magnitude of passive defect current compared to intrinsic I_{DDQ} increases, CR approaches 1. Use of a high threshold alone for CR would pass such devices. To reject such chips it is necessary to set a lower threshold for CR. This is extremely difficult due to the steepness of the low end of the CR distribution, as shown in Figure 9.

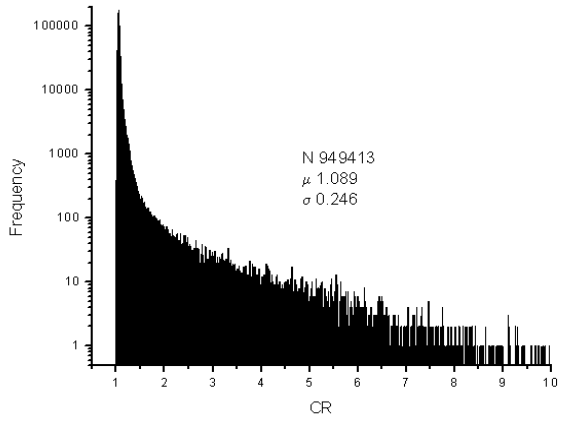

Figure 7. Distribution of CR of chips shown in Figure 6.

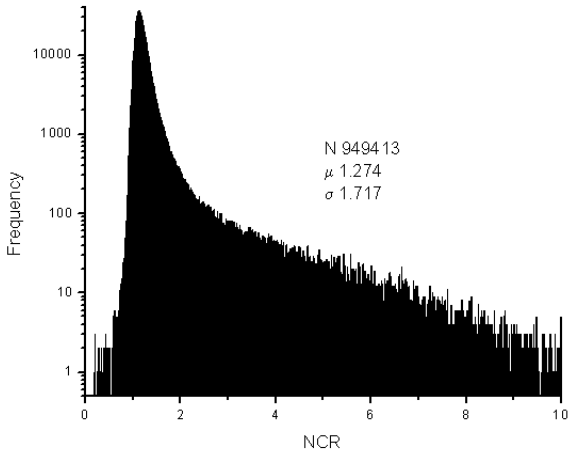

Figure 8. Distribution of NCR of chips shown in Figure 6.

Chips with a passive defect are likely to have high NCR since the probability that all neighboring chips have similar defective current for *all* vectors is extremely small. The distribution of NCR for chips having CR less than 1.02 (6909 total) is shown in Figure 10. Some of these chips must be passive defects and (assuming at least one fault-free neighboring vector) appear in the tail of the NCR distribution. A total of 447 chips show NCR above 6.5. Rejecting chips with passive defects is relatively easier with NCR. Chips with low NCR and low CR are likely fast chips. Of course, threshold setting is still a challenge. It is also possible to set a lower NCR limit for low CR devices, on the assumption that they are already suspicious. As shown in Figure 10, devices with NCR above 2 or 3 appear to be outliers.

Since NCR is a relative metric, the reliability of its prediction depends on the degree of correlation between the chip and its neighbors. When a defective chip is surrounded by fault-free chips NCR provides a reliable (conclusive) answer for accepting or rejecting an otherwise suspicious chip. Unfortunately, any relative metric can be misled by the presence of outliers in the data. Many defects on a wafer are known to form clusters [21]. Thus if the neighboring chips are defective, NCR can mislead the outlier rejection, thereby increasing test escapes. But since maximum value of NCR is used, this can only happen if all neighbors are similarly defective. Studies of systematic wafer-level variation can be helpful [16][22] to identify neighboring chips that are better estimators. Note that these chips need not be adjacent and could be at longer distances. Further, note that NCR alone is not capable of screening all outliers (see Figures 5 and 6), although there is a high probability that a CR outlier is also an NCR outlier. Therefore, CR and NCR should be used together. Correlating additional parameters can improve confidence or resolve disagreement between two metrics [18][23].

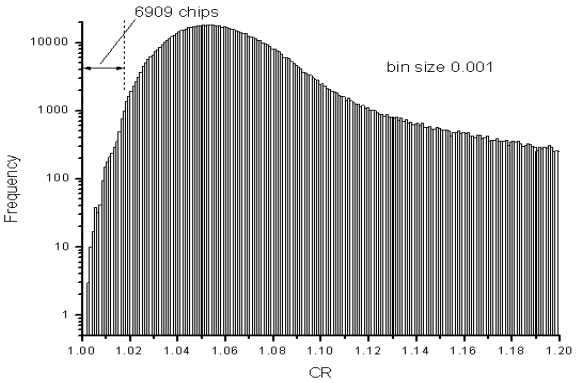

Figure 9. Distribution of CR in 1-1.02 range.

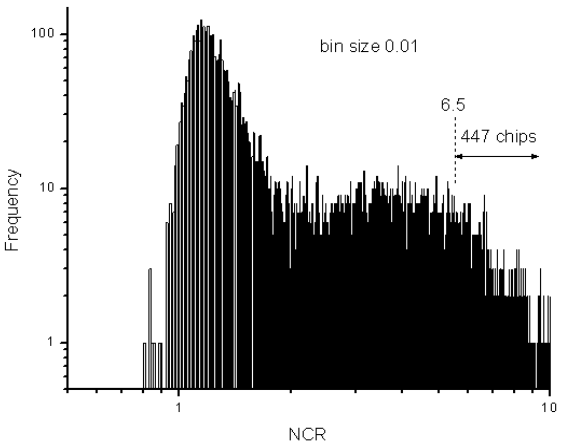

Figure 10. Distribution of NCR for chips having CR < 1.02.

5. Empirical Analysis of Industrial Data

Combining both CR and NCR provide some insights regarding both intra-die and inter-die variance in I_{DDQ}. A

chip with a passive defect would exhibit smaller CR than a fault-free chip or a chip with an active defect. Whether to screen passive defective chips or not depends on the reliability requirements. On the other hand an active defect would increase the CR. The actual increase in CR, of course, depends on the relative magnitudes of the intrinsic leakage and the defect current. The real challenge is differentiating variation in CR due to process variation from that due to a defect. This can be achieved by combining NCR with CR.

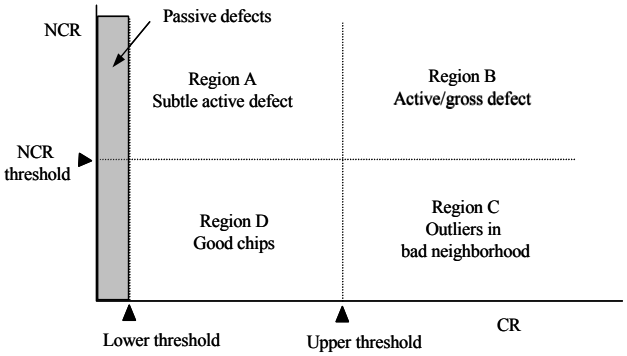

Figure 11. Categorization of chips based on CR and NCR.

Using both CR and NCR, chips can be divided into different categories as shown in Figure 11. Chips having very small CR values (close to 1) are shown as 'passive defects'. Chips having CR and NCR smaller than their maximum permissible threshold are denoted as 'Good chips' in region D. Of course, some of these chips will contain faults that do not cause elevated I_{DDQ}.

Certain subtle active defects will cause higher NCR even though their CR may not increase. Such chips fall in region A. In case of a strong active defect, both CR and NCR values are high. Such chips fall in region B. As mentioned earlier, NCR may not be very effective for screening chips that are surrounded by many defective chips. However, it is unlikely that all the neighboring chips have similar defective currents for all input vectors. Outliers in a bad neighborhood and in a fast wafer region would appear in region C. Previous studies have shown such chips to be a reliability risk [24].

Findings from SEMATECH data

We used SEMATECH data to confirm our hypothesis underlying the categorization shown in Figure 11. We considered SEMATECH test chips [25] that passed all tests or failed only I_{DDQ} test at the wafer level (12128 chips). The chips having leakage current of more than 100 μA were considered gross outliers and discarded [18]. NCR values were computed by considering all 195 vectors for each available neighbor that passed all wafer tests or failed only I_{DDQ} test and the maximum of NCR values was used. The distributions of CR and NCR values are shown in Figure 12. The gross CR and NCR outliers were discarded before plotting these distributions. As the distributions fall off very quickly after 1σ, the CR and NCR thresholds were selected (μ+σ) as 4.81 and 5.67, respectively. These thresholds are not shown in Figure 5. A lower CR threshold of 1.1 was selected so that none of the all-pass chips from the burn-in sample are in the 'passive defect' region in Figure 11. The distribution of chips in five categories (passive, A, B, C, D) is shown in Table 2.

Table 2. Distribution of SEMATECH chips.

Category (1941BI + 10187 no BI)	Wafer Probe Result		Post BI Result
	All Pass (11220)	I_{DDQ} Fail (908)	
Passive Defects (33+7)	-	-	All Pass
	-	31	I_{DDQ} Fail
	-	2	Boolean Fail
	1	6	No BI
Region A (337+465)	55	86	All Pass
	3	184	I_{DDQ} Fail
	2	7	Boolean Fail
	447	18	No BI
Region B (551+416)	48	119	All Pass
	5	369	I_{DDQ} Fail
	-	10	Boolean Fail
	380	36	No BI
Region C (19+125)	14	1	All Pass
	-	3	I_{DDQ} Fail
	-	1	Boolean Fail
	125	-	No BI
Region D (1001+9174)	935	19	All Pass
	19	11	I_{DDQ} Fail
	17	-	Boolean Fail
	9169	5	No BI

Figure 13 shows the current signature [5] for a sample chip from the SEMATECH data from each of five regions shown in Figure 11. Notice that chips in regions A, B and C all show the presence of an active defect with a varying degree of severity. The chip from region D shows a smooth fault-free signature. A die with a passive defect also shows similar smooth signature.

The SEMATECH burn-in test data can give us some insight about the reliability of the chips in the different regions. Chips in regions A, B, C and the passive defects are assumed to be fatally flawed and rejected. Chips in region D are assumed to be good. The defect level (DL) of the shipped lot (region D) and the yield loss (YL) incurred for rejecting the other regions are computed by using the following equations:

$$DL = \frac{Number\ of\ post-BI\ Boolean\ fails}{Total\ number\ of\ chips\ in\ the\ category} * 100$$

$$YL = \frac{Number\ of\ chips\ that\ pass\ all\ tests\ at\ both\ levels}{Total\ number\ of\ chips\ in\ the\ category} * 100$$

Chips that pass all tests at both levels

Since the SEMATECH definition of "all pass" implied I_{DDQ} less than 5 μA, a majority of all pass chips have small

CR and NCR values as shown in Figure 14. However, it is interesting to note that some chips exhibit high CR and/or NCR. Even though these chips did pass all tests, they are a potential reliability risk. This underscores the fact that thresholds are getting fuzzier and "different behavior" is reason enough to reject chips [26].

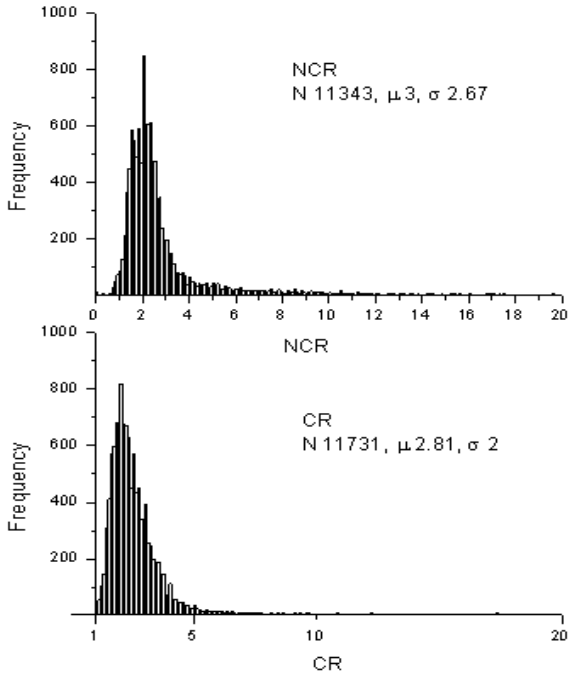

Figure 12. Distributions of CR and NCR values less than 20.

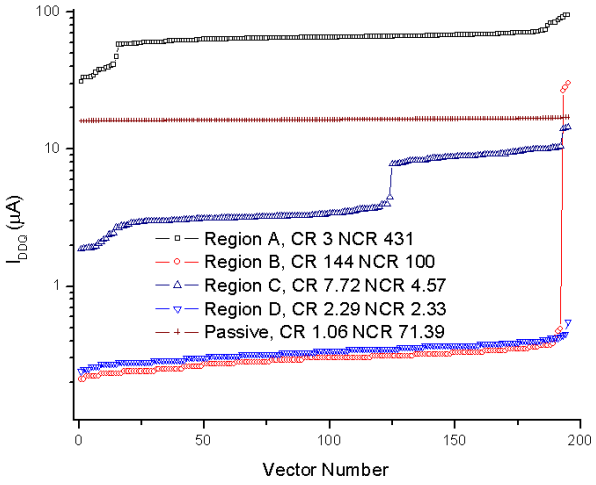

Figure 13. Current signatures for die from regions shown in Figure 11.

Chips that failed only I_{DDQ} test at wafer and post-BI test are considered either faulty or fault-free. Healer chips are considered defective. The results were then scaled up to the entire population based on the distribution of chips used in the BI sample. There are too few passive defects or region C chips to perform an analysis and so are not considered further. The results of the analysis are shown in Table 3. The results support our hypothesis that chips from region B are more likely to be defective than chips from other regions, but chips from region A also have a high defect level.

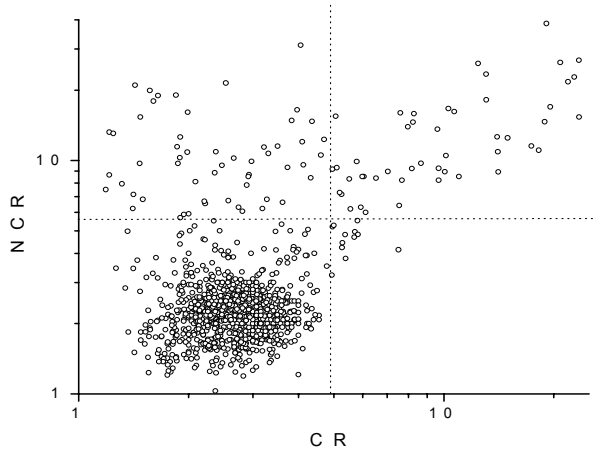

Figure 14. CR/NCR scatter plot for chips that passed all tests before and after burn-in.

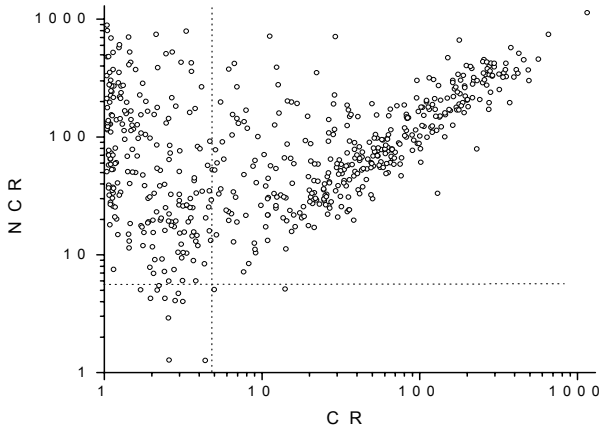

Figure 15. CR/NCR scatter plot for chips that failed only I_{DDQ} test before and after burn-in.

Table 3. Defect level and yield loss for various categories.

Category	Defect Level (%)		Yield Loss (%)
	I_{DDQ} fail = Fault-free	I_{DDQ} fail = Faulty	
Region A	3	58	15.9
Region B	1.8	69	8.38
Region D	1.69	4.69	NA

It is interesting to see the trends in CR and NCR values of the following sub-categories: chips that pass all tests at both levels, chips that fail only I_{DDQ} test at both levels and chips that fail Boolean test after BI (independent of their wafer probe result). Figures 14 through 16 show CR/NCR scatter plots of these chips.

Chips that fail only I_{DDQ} test

The I_{DDQ} threshold of 5 μA was decided by empirical analysis and does not represent a good manufacturing limit [15]. Understanding the behavior of chips that fail only I_{DDQ}

test has been a topic of interest [27] due to yield loss [28] as well as reliability issues [29], the latter becoming more important with technology scaling. SEMATECH chips show strange behavior in this regard. Chips spread over several orders of magnitude of NCR fail only I_{DDQ} test (see Figure 15). Most of these chips are in regions A and B and are likely to have active defects as depicted by current signatures in Figure 13. Some of these chips may exhibit healing behavior later after extended burn-in [30], but for all practical purposes, these chips are a reliability risk and must be rejected up front in the test flow. Since such rejection at the wafer level in burn-in avoidance mode can result in excessive yield loss, the thresholds for CR/NCR must be appropriately selected.

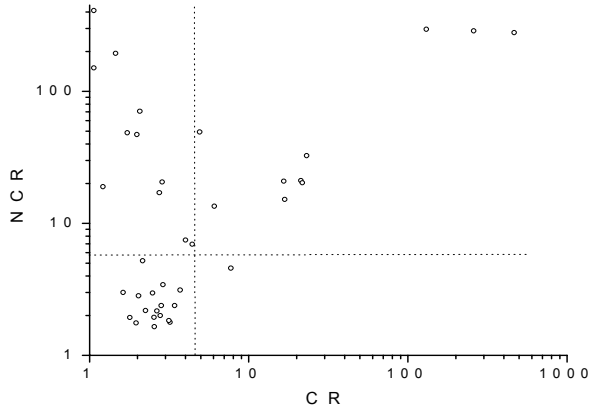

Figure 16. CR/NCR scatter plot for chips that failed Boolean test after burn-in.

Chips that fail Boolean test after burn-in

Figure 16 shows the CR/NCR scatter plot for chips that fail a Boolean test after burn-in. Such chips from region A generally have high NCR. This can occur if a chip has multiple active defects or a combination of active and passive defects resulting in a shift in I_{DDQ} values, while limiting CR.

Chips that fail Boolean tests from region D exhibit random variation in NCR. A similar random nature is also observed for chips from region B. Unfortunately the SEMATECH burn-in sample was biased and the data set is too limited to draw meaningful conclusions in this regard. Some of the defects that lead to these Boolean fails are not I_{DDQ}-testable and, therefore, CR/NCR values are close to their mean values.

6. Conclusions and Future Work

With increasing background leakage it is necessary to adopt statistical means and correlation with other process parameters to sustain I_{DDQ} test in future technologies. Deciding an appropriate CR threshold is difficult due to the several orders of magnitude variation in fault-free I_{DDQ}. Therefore, it is necessary to use secondary information to identify outliers. This paper proposes a combination of two I_{DDQ} test metrics for screening outlier chips by exploiting wafer-level spatial correlation. No single metric alone is sufficient to screen all outliers. The addition of a second degree of freedom also comes at the risk of additional yield loss. The thresholds for two metrics must be carefully selected to optimize yield loss/defect level. Use of additional test parameters (e.g. chip speed) might be useful to sort out the disagreement between two metrics. Whether the accompanying reduction in the defect level is appropriate is left to a semiconductor manufacturer's discretion.

Maintaining stringent process control will prove to be challenging for DSM technologies. Understanding underlying process variables and their impact on test parameters will be crucial for yield requirements. As I_{DDQ} test loses its effectiveness, it will be necessary to correlate multiple test metrics in the future. A combination of multiple outlier screening methods may be needed [31]. Scalability of the metrics used for outlier rejection will be crucially important. The basic physical mechanisms that govern CR and NCR will not change in the future. Therefore, the CR/NCR combined metric should be scaleable to future technologies. NCR is not a variance reduction technique like other methods [10]. However, a combination of CR/NCR with other test parameters can be useful for screening low-reliability chips. It will be interesting to see whether the variation in CR/NCR thresholds helps screen chips with different severities of defect currents. We did not investigate the relationship between the vector pairs yielding CR and NCR. It will be interesting to examine if such correlation exists and whether that can be useful for production implementation of NCR-based outlier rejection. Analysis of wafer patterns can be useful to reduce number of vector pairs that may be required [16][32].

Acknowledgements

This research was funded in part by the Texas Advanced Research Program under grant 512-186-2001 and by Semiconductor Research Corporation under grant 2001-TJ-954. Thanks to Phil Nigh (IBM) and Kevin Cota, Bob Madge and Manu Rehani (LSI Logic Corporation) for data. The conclusions drawn are our own and do not necessarily represent the views of IBM or LSI Logic.

References

[1] *Intl. Technology Roadmap for Semiconductors* (ITRS), Semiconductor Industry Association, 2001 [online] http://public.itrs.net.

[2] T. W. Williams et al., "I_{DDQ} Testing for High Performance CMOS – the Next Ten Years," *European Design and Test Conf.*, Paris, France, Mar. 1996, pp. 578-583.

[3] T. W. Williams et al., "I_{DDQ} Test: Sensitivity Analysis of Scaling," *IEEE Intl. Test Conf.*, Washington DC, Oct. 1996, pp. 786-792.

[4] M. Sachdev, "Deep Sub-micron I_{DDQ} Testing: Issues and Solutions," *European Design and Test Conf.*, Paris, France, Mar. 1997, pp. 271-278.

[5] A. Gattiker and W. Maly, "Current Signatures: Application," *IEEE Intl. Test Conf.*, Washington DC, Oct. 1997, pp. 156-165.

[6] C. Thibeault, "Improving Delta- I_{DDQ} -based Test Methods," *IEEE Intl. Test Conf.*, Atlantic City, NJ, Oct. 2000, pp. 207-216.

[7] P. Maxwell et al., "Current Ratios: A Self-scaling Technique for Production I_{DDQ} Testing," *IEEE Intl. Test Conf.*, Atlantic City, NJ, Oct. 1999, pp. 738-746.

[8] S. Jandhyala et al., "Clustering Based Techniques for I_{DDQ} Testing," *IEEE Intl. Test Conf.*, Atlantic City, NJ, Oct. 1999, pp. 730-737.

[9] P. N. Variyam, "Increasing the I_{DDQ} Test Resolution Using Current Prediction," *IEEE Intl. Test Conf.*, Atlantic City, NJ, 2000, pp. 217-224.

[10] W. R. Daasch et al. "Variance Reduction Using Wafer Patterns in I_{DDQ} Data," *IEEE Intl. Test Conf.*, Atlantic City, NJ, Oct. 2000, pp. 189-198.

[11] S. Sabade and D. M. H. Walker, "Improved Wafer-level Spatial Analysis for I_{DDQ} Limit Setting," *IEEE Intl. Test Conf.*, Baltimore, MD, Oct. 2001, pp. 82-91.

[12] Y. Okuda, "DECOUPLE: Defect Current Detection in Deep Submicron I_{DDQ}," *IEEE Intl. Test Conf.*, Atlantic City, NJ, 2000, pp. 199-206.

[13] D. Bergman and H. Engler, "Improved I_{DDQ} Testing with Empirical Linear Prediction," *IEEE Intl. Test Conf.*, Baltimore, MD, Oct. 2002, pp. 954-963.

[14] J. Diez and J. Lopez, "Influence of Manufacturing Variations in I_{DDQ} Measurements: A New Test Criterion," *Design and Automation Test Conf.*, Los Angeles, CA, June 2000, pp. 645-649.

[15] P. Nigh et al., "So What is an Optimal Test Mix? A Discussion of the SEMATECH Methods Experiment," *IEEE Intl. Test Conf.*, Washington DC, Oct. 1997, pp. 1037-1038.

[16] R. Daasch et al., "Neighbor Selection for Variance Reduction in I_{DDQ} and Other Parametric Data," *IEEE Intl. Test Conf.*, Baltimore, MD, Oct. 2001, pp. 92-100.

[17] S. Sabade and D. M. H. Walker, "Neighbor Current Ratio (NCR): A New Metric for I_{DDQ} Data Analysis," *IEEE Intl. Symp. on Defect and Fault Tolerance in VLSI Systems*, Vancouver, Canada, Nov. 2002, pp. 381-389.

[18] S. Sabade and D. M. H. Walker, "Wafer-level Spatial and Flush Delay Correlation Analysis for I_{DDQ} Estimation," *IEEE Intl. Workshop on Defect Based Testing*, Monterey, CA, Apr. 2002, pp. 47-52.

[19] J. R. Taylor, "An Introduction to Error Analysis," *University Science Books,* 1982.

[20] Ronald Richmond, "Successful Implementation of Structured Testing," *IEEE Intl. Test Conf.,* Atlantic City, NJ, Oct. 2000, pp. 344-348.

[21] A. D. Singh and C. M. Krishna, "On the Effect of Defect Clustering on Test Transparency and IC Test Optimization," *IEEE Trans. on Computers*, Vol. 45. No. 6, June 1996, pp. 753-757.

[22] R. Madge et al., "Statistical Post-Processing at Wafersort – An Alternative to Burn-in and a Manufacturable Solution to Test Limit Setting for Sub-micron Technologies," *IEEE VLSI Test Symp.,* Monterey, CA, Apr. 2002, pp. 69-74.

[23] A. Keshavarzi et al., "Multiple-Parameter CMOS IC Testing with Increased Sensitivity for I_{DDQ}," *IEEE Intl. Test Conf.*, Atlantic City, NJ, Oct. 2000, pp. 1051-1059.

[24] A. D. Singh et al., "Screening for Known Good Die Based on Defect Clustering: An Experimental Study," *IEEE Intl. Test Conf.,* Washington DC, 1997, pp. 362-369.

[25] P. Nigh et al., "An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, I_{DDQ} and Delay-Fault Testing," *IEEE VLSI Test Symp.,* Monterey, CA, May 1997, pp. 459-464.

[26] P. Maxwell, "The Heisenberg Uncertainty of Test," Invited Address*, IEEE Intl. Test Conf.,* Baltimore, MD, Oct. 2002, p. 13.

[27] A. Gattiker and W. Maly, "Toward Understanding I_{DDQ}-Only Fails," *IEEE Intl. Test Conf.*, Washington DC, 1998, pp. 174-183.

[28] S. Davidson, "Is I_{DDQ} Yield Loss Inevitable?," *IEEE Intl. Test Conf.*, Washington DC, Oct. 1994, pp. 572-579.

[29] C. Hawkins et al., "Reliability, Test and I_{DDQ} Measurements," *IEEE Intl. Workshop on I_{DDQ} Testing*, Washington DC, 1997, pp. 96-102.

[30] A. Gattiker et al., "Current-Signature-Based Analysis of Complex Test Fails," *Intl. Symp. on Test and Failure Analysis*, Santa Clara, CA, 1999, pp. 377-387.

[31] R. Madge et al., "Screening $MinV_{DD}$ Outliers Using Feed-Forward Voltage Testing," *IEEE Intl. Test Conf.,* Baltimore, MD, Oct. 2002, pp. 673-682.

[32] R. B. Miller and W. C. Riordan, "Unit Level Predicted Yield: a Method of Identifying High Defect Density Die at Wafer Sort," *IEEE Intl. Test Conf.*, Baltimore, MD, 2001, pp. 1118-1127.