# On Comparison of NCR Effectiveness with a Reduced I<sub>DDQ</sub> Vector Set

Sagar Sabade

D. M. H. Walker

Department of Computer Science Texas A&M University College Station, TX 77843-3112 Phone: (979) 862-4387 Fax: (979) 847-8578 E-mail: [sagars, walker]@cs.tamu.edu

### Abstract

 $I_{DDQ}$  test-based outlier rejection becomes difficult for deep sub-micron technology chips due to increased leakage and process variations. The use of Neighbor Current Ratio (NCR) that uses wafer-level spatial correlation for identifying outlier chips has been proposed earlier as a means of coping with these issues. Due to the slow speed of  $I_{DDQ}$  test, there is a strong motivation to reduce the number of test vectors without compromising the fault coverage. In this paper, we examine the effectiveness of Neighbor Current Ratio using a reduced  $I_{DDQ}$  vector set and industrial test data.

# 1. Introduction

Advances in semiconductor manufacturing process technology permit higher chip performance by shrinking transistor geometries. However, as transistors become smaller, it is necessary to scale both the supply and threshold voltages [1]. This results in an exponential increase in transistor leakage current ( $I_{DDQ}$ ) [2]. In addition, increased process variations results in large inter-die variation in  $I_{DDQ}$ . This makes distinguishing faulty and fault-free  $I_{DDQ}$  difficult [3]. Due to rising background currents in deep sub-micron (DSM) chips, it is difficult to discriminate faulty  $I_{DDQ}$  current [4][5]. Hence,  $I_{DDQ}$  testing is considered a difficult challenge by the International Technology Roadmap for Semiconductors (ITRS) [6].

One solution to this problem is to reduce the leakage current [7]. Though this extends the usability of  $I_{DDQ}$  test in the DSM era, it does not solve the problem completely. Therefore, leakage reduction techniques need to be accompanied by statistical post processing of data. These methods attempt to estimate fault-free  $I_{DDQ}$  variation to make faulty values distinguishable. These include use of statistical methods, graphical display of data, and use of correlation between  $I_{DDQ}$  of neighboring dice [8]-[13].

Due to underlying process variations, there exists strong wafer-level spatial correlation between different die positions on a wafer. This correlation can be used for estimating fault-free parameters [11][12] in order to identify outlier chips [14][15]. Since there is no fault-free mechanism that can explain an abrupt variation in  $I_{DDQ}$  of two neighboring dice, the higher  $I_{DDO}$  must be due to a

defect. This forms the basic philosophy behind outlier identification using spatial correlation. It has been shown that the Neighbor Current Ratio (NCR) metric is capable of detecting some passive or pattern-independent defects (e.g. a resistive short between power supply lines) that are not caught by other test methods such as Current Ratio (CR) [16]. Although passive defects do not change the functionality of a circuit, they increase power consumption and can result in low reliability. Since passive defects elevate I<sub>DDQ</sub> for a chip independent of the input, even a single vector should be sufficient for detecting a defect provided leakage current is sufficiently large and the test method used is sensitive to such defects.

One of the limitations of  $I_{DDQ}$  test is its relatively slow test speed. The use of faster  $I_{DDQ}$  measurement [17][18] and/or change of sequence of test vectors [19] are possible alternatives, but they are sometimes design-specific. Hence, there is a strong motivation for screening defective chips with a reduced  $I_{DDQ}$  vector set. In this paper, we examine the effectiveness of the NCR test metric in combination with CR for detecting passive defects with a reduced vector set. The remainder of this paper is organized as follows. In the next section, we briefly describe the CR concept and review the NCR metric. In Section 3, we evaluate the effectiveness of CR and NCR with a reduced vector set. Section 4 presents empirical analysis of industrial test data. Section 5 presents discussion and finally Section 6 concludes the paper.

# 2. Review of CR and NCR

In its simplest form, CR is defined as the ratio of the maximum to the minimum  $I_{DDQ}$  of a chip. Since process variations are relatively uniform across chips, the increase in the leakage current is expected to be proportionate. Therefore, if the increase in leakage current is solely due to process variations, the CRs are similar for fault-free chips. This is illustrated in Fig. 1. It shows two chips having different *magnitudes* of current but proportionately similar within-chip *variance* in  $I_{DDQ}$ . The presence of an active or pattern-dependent defect (e.g. a short between two signal lines) violates this assumption and results in a high CR. The presence of a passive defect causes reduced CR as  $I_{DDQ}$  is elevated for all vectors. These two cases are shown in Fig. 2. Chip 1 has an active defect as indicated by a large jump

in its current signature [10] and has a higher CR than nominal ( $\sim$ 1.2). Chip 2 has a passive defect and therefore has a smaller than nominal CR. This example illustrates that unless a lower CR threshold is used, screening passive defects is not possible with CR. Setting a lower CR threshold to screen such defects is difficult due to the steep distribution and can result in excessive yield loss [20].



Fig. 1. Process variation yields similar CRs.



Fig. 2. CR for chips with active and passive defects.



Fig. 3. Wafer-level spatial variation in I<sub>DDO</sub>.

#### Use of wafer-level spatial variation

We proposed the Neighbor Current Ratio (NCR) test metric that can improve the defect-screening resolution of  $I_{DDQ}$  test. [15]. The NCR metric relies on wafer-level spatial correlation. It is based on the observation that neighboring dice on a wafer undergo similar process fluctuations. Hence, their fault-free  $I_{DDQ}$  values are *similar* with the ratio close to 1. Fig. 3 shows  $I_{DDQ}$  values for all chips on a wafer for a vector. Notice that except for some spatial outliers, the variation in  $I_{DDQ}$  across the wafer is smooth. NCR is based on this observation.

NCR is defined as the ratio of  $I_{DDQ}$  of a die to that of its neighboring die for the *same* vector. Note that for CR the vector is the variable while for NCR, the chip is the variable factor. Only fault-free neighboring dice are considered for NCR computation. With N immediate neighbors and k vectors per die, a total of N-k NCR values can be computed for each die. For outlier screening, the maximum of all NCR values is used as it shows the maximum nonconformance of a die to its neighborhood. Henceforth, NCR refers to the maximum of all NCRs.



Fig. 4. Wafer-level spatial variation in CR.



Fig. 5. Wafer-level spatial variation in NCR.

The original definition of NCR as described in [14]-[16] considers only immediate neighboring dice. That is, only eight adjacent positions can be considered. It is possible to

extend the neighborhood definition to longer distances [11] or to die positions that show strong correlation [21]. However, in this work we restrict ourselves to the original definition.

Fig. 4 shows a wafer surface plot of CRs for each die. Notice that CR variation across the wafer is smoother than the I<sub>DDO</sub> variation in Fig. 3, thus supporting the CR concept. The chips with active defects appear as peaks or spatial outliers. The wafer surface plot of NCR values for the same wafer is shown in Fig. 5. The following observations can be made. First, the variation for NCR is larger than that observed for CR in Fig. 4. This is because we consider the maximum of all NCR values and the NCR computation uses more vectors than CR alone. Secondly, for some chips NCR values are actually lower than CR values. These chips either are in a bad neighborhood or conform to local process variations. Chips having higher NCR but smaller CR are most likely passive defects or a subtle active defect dominated by passive defect current. Earlier we have shown that a combination of CR and NCR can be used for distinguishing between different defect types [22]. It is possible to use different thresholds for CR and NCR depending on the defect severity.



Fig. 6. CR distributions for different vector lengths.

### 3. Reduced Vector Set NCR

Test, in a broader sense, is an optimization problem. Manufacturers wish to catch the *maximum* defective chips with the *minimum* test cost. The minimum test cost is achieved by using a shorter or better test or reducing test time. There are several reasons for using a small set of vectors for  $I_{DDQ}$  test.  $I_{DDQ}$  may be performed after stuck-at or functional tests and only to screen parts that are *deemed* defective. Due to high observability of  $I_{DDQ}$  a small number of vectors may be enough to achieve adequate fault coverage. Secondly,  $I_{DDQ}$  can be measured only after internal circuit switching is settled. This makes  $I_{DDQ}$  a relatively slow test. Thus, a smaller number of vectors reduces overall test time.

Manufacturers wish to optimize test time without compromising defect level (DL) targets. Defect detection probability depends on the controllability and observability conditions for the fault site and the number of vectors. For I<sub>DDQ</sub> test, the observability condition is always met as power supply lines can always be monitored. If the defect is passive, it should get detected with a single vector assuming the I<sub>DDQ</sub> is larger than the pass/fail threshold. This is especially true with NCR since we consider the maximum NCR value and a passive defect in a good neighborhood always appears as a spatial outlier. For active defects, defect detection depends on the excitation probability. Its value increases as the number of vectors increases. That is, DL and test length have a reciprocal relationship. The DL saturates after a certain test length as faults become harder to detect. We are interested in observing the effective change in DL due to a reduced vector set while using CR and NCR.

We use data from LSI Logic and Texas Instruments (TI) for our evaluation of these methods. The LSI Logic data contains a total of 931119 chips from 79 lots and 1342 wafers for 180 nm technology. For each chip, 20 I<sub>DDO</sub> readings are available. The TI data contains 7251 chips from 7 lots and 26 wafers for 130 nm technology. For each chip, 12 I<sub>DDQ</sub> readings are available. For both manufacturers, I<sub>DDO</sub> pass/fail thresholds are not known. We considered a smaller subset of vectors (in steps of 4 or 5) for CR and NCR computation. Thus, for LSI data we initially considered the first 5 vectors, then increased the vector length in steps of 5. Fig. 6 shows how the CR distribution changes when additional vectors are considered. In this figure, 699 chips from a wafer are shown. A chip whose CR increases from 1.2 to over 2 (off the scale in (d)) is marked with the arrow. Also, notice the gradual shift in skew of the distribution that changes from negative to positive from (a) to (d) as CR increases for chips in the main body. This is due to state-dependent variation in I<sub>DDO</sub>. The chips with active defects or a combination of active and passive defects appear in the main body of the distribution until a vector that excites them is reached. Once this vector is reached, these chips move from lower CR values to the right side of the distribution. For the same chips, the distribution for the NCR values is shown in Fig. 7. The distribution does not show any noticeable shift with increasing number of vectors. This is because passive defects are mostly in the tail of the distribution with the first few vectors. The changes in the main body of the distribution are due to vector-to-vector variation across chips. Chips with an active

defect show movement similar to CR. However, it appears that the distribution is mostly populated by passive defects.

A shift in CR/NCR values is noticeable for some chips in the TI data as shown in Fig. 8. A chip marked in the figure contained a gross active defect that was excited by one of the last 8 vectors. Note that this chip was already an outlier after 4 vectors. The changes in CR and NCR for this chip are marked in Fig. 8. In this case, the relative change in CR is higher than that for NCR. However, note there are many chips for which NCR changes more than CR. For some chips, this cannot be observed due to overlapping points in the plot.



Fig. 7. NCR distribution for different vector lengths.



Fig. 8. CR and NCR shift for different vector lengths.

# 4. Empirical Analysis

In order to compare the effectiveness of CR and NCR as the number of vectors is changed, we used the following approach. Since the term DL is probably misleading here, we use another term called miss rate as described later. To make a fair comparison with CR, it was necessary to set a lower threshold on CR. From our prior experiments reported in [22], we used a lower threshold of 1.02. That is we implicitly assume that chips having CR smaller than 1.02 have predominantly passive defects.

Table I. Distribution of LSI chips for different vectors sets.

| CR    | 5 vec  | 10 vec | 15 vec | 20 vec | NCR   |
|-------|--------|--------|--------|--------|-------|
| <1.02 | 191202 | 26153  | 10749  | 4546   | <1.69 |
| <1.02 | 6242   | 3638   | 2792   | 2364   | >1.69 |
| 1.02- | 730015 | 891608 | 905253 | 910247 | <1.69 |
| 1.29  | 7057   | 9091   | 9776   | 10114  | >1.69 |
| >1 20 | 7858   | 10713  | 12187  | 13086  | <1.69 |
| ~1.29 | 7040   | 8211   | 8657   | 9057   | >1.69 |

Table II. Number of chips accepted by two methods.

| Vectors | CR Accept | NCR Accept | CR/NCR<br>Accept |
|---------|-----------|------------|------------------|
| 5       | 737072    | 929075     | 730015           |
| 10      | 900699    | 928474     | 891608           |
| 15      | 915029    | 928189     | 905253           |
| 20      | 920361    | 927879     | 910247           |



Figure 9. CR and NCR distributions for the sample.

The upper threshold for CR and NCR were decided using a small sample. The distributions of CR and NCR values from this sample are shown in Fig. 9. The mean+ $3\sigma$  value for NCR is 1.69. Since the CR distribution is not Normal we used a threshold of 1.29. The upper threshold obtained by the Tukey method<sup>1</sup> for CR was 1.14 (see [23] for details on the Tukey method). Hence, the 1.29 limit was reasonably relaxed. If CR or NCR exceeded any thresholds, a chip was considered defective.

#### Calculating miss rate

We define the miss rate as the percentage of chips that are not detected by a metric compared to the full vector set. Thus, we consider the miss rate for the full vector set (20 vectors for the LSI data and 12 vectors for the TI data) to be zero. The miss rate for other vector sets is calculated as:



Figure 10. Migration of outliers in a 2D space.

# 5. Discussion

Table I shows how the distribution of LSI chips accepted by CR and NCR changes when more vectors are considered. The total number of chips accepted for different vector lengths are shown in Table II. The migration of low CR chips to the high CR category can be noticed. The change is not uniform. For example, changing the number of vectors from 5 to 10 catches more defective chips than changing it from (say) 15 to 20. This is because the initial vectors detect mostly gross defects. The migration of chips from nominal CR to other categories can be visualized in a two-dimensional space as shown in Fig. 10. The chips can move only towards the right and/or upward. Thus, it is possible that some chips move from the passive defect region (CR<lower threshold) to region D (nominal CR) or region A (NCR outlier) or, in some cases, to region B (gross outliers). This also explains why the number of chips accepted by CR can increase with the number of vectors. Chips that move from the passive region to another region appear passive only due to small intra-vector variability in I<sub>DDQ</sub>.

Table III shows how the miss rate changes when the number of vectors is changed. Compared to NCR, the change in miss rate is sharper for CR alone. Note however that our definition of miss rate is relative to the full vector set. These chips which are not caught by a reduced vector set are functional. The number of chips accepted by CR increases with increasing number of vectors because for some chips CR increases above the lower threshold but is less than the upper threshold. Some of these chips could be a combination of active and passive defects with only the later vectors exciting the active defect.

| Table III. Effective miss rate for two me |
|-------------------------------------------|
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| Vectors   |         | Miss Rate % |        |
|-----------|---------|-------------|--------|
| vectors - | CR-only | NCR-only    | CR+NCR |
| 15        | 0.58    | 0.03        | 0.55   |
| 10        | 2.18    | 0.06        | 2.09   |
| 5         | 24.86   | 0.12        | 24.68  |

For the TI data, we followed a similar approach. The thresholds for CR and NCR were 1.25 and 1.4, respectively. The lower threshold on CR was 1.05. Table IV shows the distribution of chips for different vectors, Table V shows the total number of chips accepted by each metric and Table VI shows the effective miss rate for each metric.

The TI data shows somewhat different behavior than the LSI data. Increasing vector count increases the CR of many chips above the upper threshold. Hence, fewer chips are accepted by CR as the number of vectors increase.

Table IV. TI data distribution for different vector lengths.

| CR    | 4 Vec | 8 Vec | 10 Vec | 12 Vec | NCR  |
|-------|-------|-------|--------|--------|------|
| <1.05 | 255   | 221   | 210    | 203    | <1.4 |
|       | 20    | 17    | 17     | 16     | >1.4 |
| 1.05- | 5879  | 5306  | 5124   | 5001   | <1.4 |
| 1.25  | 90    | 86    | 83     | 83     | >1.4 |
| >1.25 | 935   | 1521  | 1711   | 1840   | <1.4 |
|       | 72    | 100   | 106    | 108    | >1.4 |

Table V. Chips accepted and rejected by CR and NCR.

| Vectors | Accepted by CR | Accepted by NCR | Accepted by both |
|---------|----------------|-----------------|------------------|
| 4       | 5969           | 7069            | 5879             |
| 8       | 5392           | 7048            | 5306             |
| 10      | 5207           | 7045            | 5124             |
| 12      | 5084           | 7044            | 5001             |

Table VI. Effective miss rate for two methods.

| Vectors   |         | Miss Rate % | )      |
|-----------|---------|-------------|--------|
| vectors — | CR-only | NCR-only    | CR+NCR |
| 10        | 2.36    | 0.01        | 2.4    |
| 8         | 5.71    | 0.05        | 5.74   |
| 4         | 14.82   | 0.35        | 14.93  |

 $<sup>^{1}</sup>$  Q1 = 1.064, Q3 = 1.089, IQR = 0.025, median = 1.07, LQL = 0.995, UQL = 1.145.

The effective change in the miss rate will depend on whether active or passive defects are more dominant. There is no improvement in the miss rate when using NCR when the defective population is dominated by active defects. LSI and TI data show different migration of outliers with changing vectors. Using CR alone results in high miss rate for LSI data. For TI data, a few chips show "passive defect" behavior. Hence, the addition of NCR improves yield but does not cause a drastic change in the miss rate.

#### 6. Conclusions and Future Work

The use of spatial information is useful for spotting some outliers that are not detected by CR alone. Our prior research has shown that neither metric alone is sufficient and is supported in this work. NCR is a relative metric Therefore defective chips in a bad neighborhood cannot be screened effectively. In this work, we investigated whether reducing the number of vectors has similar miss rates on CR and NCR. The actual rates depend on the active and passive defect distribution. The main advantage of NCR comes from detection of chips that have passive leakage component.

We also observed that it is necessary to use an "adequate" number of vectors. This number depends on several factors including defect detection capability of each vector, current resolution, etc. This is especially true for the CR metric. A better outlier screening may be possible by increasing the neighborhood window. The NCR definition can be extended to die positions that are highly correlated on a wafer, similar to that suggested in [21].

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