Title of Invention:
Current Sensor System to Measure Integrated Circuit Quiescent Current (IDDQ)

Name, Department and System Component of each Inventor:
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1. State in general terms the purpose of the invention. Is it a new product, process or composition of matter? A new use for or improvement to an existing product, process or composition of matter?

   This invention proposes a current sensor system that can measure the quiescent current (IDDQ) of an integrated circuit (IC) with high resolution and high speed. We term this an IDDQ sensor. The IDDQ sensor circuitry is compatible with standard digital semiconductor technology, so the sensor can be fabricated on the same chip as the circuit that it is sensing. When using multiple sensors within an IC, the IC power supply network can be partitioned so that the background leakage current is reduced to a level such that small changes in IDDQ can be detected. This permits the screening of many defective parts in IC manufacturing test, both at the wafer and package level. The small size and power consumption of the invention permits a large number of partitions to be used. This permits the user to keep the background leakage current small even as the total IC background leakage current rises rapidly with each semiconductor manufacturing technology generation. The high speed and parallel measurement capabilities permit large numbers of current sensors to be used with economical test times. The invention indirectly measures the IDDQ without disturbing the performance of the IC in normal operation, permitting the invention to be used in high-speed integrated circuits. The combination of the high-resolution IDDQ sensor and partitioning provides diagnosability so that a defect within the IC that causes elevated IDDQ can be isolated to a partition.

   The invention measures the IDDQ indirectly by measuring the magnetic field generated by the IDDQ, digitizing it, and scanning it out via a scan chain (a shift register). The invention consists of the following components: MAGFET sensor, stochastic sensor with self-calibration
tool, data detector, and counter/scan register. The MAGFET sensor component measures the
IDDQ by using the Lorentz force exerted on moving carriers by the magnetic field generated by
current flowing from VCC to VSS when the IC is in a quiescent state (the IDDQ current
component). The MAGFET sensor uses an arrangement of cross-coupled, split-drain MAGFETs to
convert this force into a voltage difference. This voltage is converted to a digital bit stream using
the stochastic sensor component and data detector. This bit stream is counted in the counter/scan
register component. The resulting count can be scanned out to provide a digital reading of the
IDDQ value. The self-calibration tool within the stochastic sensor is used to correct for any offset
in the IDDQ sensor, so that a zero IDDQ current results in a very small digital value. The reference
current within the MAGFET sensor is used to compute the gain of the system so that the digital
value can be translated into an IDDQ current value.
2. **Identify features, which are believed to be new, unexpected or critical.**

IDDQ current measurement is widely used to detect defects in ICs that occur during semiconductor fabrication. The conventional method is to measure the IDDQ current directly by inserting the measurement tool between the power supply and the IC VCC connections, or between the IC VSS connections and the power supply, and measure a voltage drop across the sensor within the tool. Inserting the measurement tool leads to performance degradation during normal IC operation and longer testing time. This invention avoids performance degradation and low test speed by indirectly measuring the IDDQ by measuring the magnetic field generated by the IDDQ current. Its digital readout capability, high speed, small size, and ability to operate in parallel with other sensors permits the use of large numbers of sensors on a chip with the supply network partitioning method. This is necessary to achieve high IDDQ measurement resolution in modern semiconductor technologies with economical testing times.

The MAGFET sensor generates a very small voltage signal for the IDDQ current values of interest. Furthermore, the inherent noise of the sensor is much larger than the signal. To convert this signal reliably into a digital value, a stochastic sensor is used in combination with a data detector and counter/scan register. Unlike other analog-to-digital conversion (ADC) methods, this arrangement relies on the noise being larger than the signal. Also unlike other ADC methods, the stochastic sensor and counter/scan register can be built reliably in a typical digital semiconductor fabrication technology, and has a small size. Both the MAGFET sensor and stochastic sensor can have offset values much larger than the signal generated by the IDDQ current, that preclude correct IDDQ sensor operation. These offsets result from manufacturing variations. A self-calibration tool within the stochastic sensor minimizes this offset prior to IDDQ measurements. A self-calibration tool is essential for practical operation since calibrating multiple IDDQ sensors on a chip one at a time would take an excessively long time. The reference current within the MAGFET sensor permits translation of digital values to IDDQ current values. This is essential since circuit specifications are given in actual current values. Placing two different current values on the reference current line and measuring the resulting digital values permits computation of the gain of the IDDQ sensor in terms of change in digital value for a change in IDDQ current. The reference current is also essential since the gain is a function of the inherent sensor noise, which is a dependent on manufacturing variations.
The IDDQ sensor can measure IDDQ current flowing in either direction through the sensor. This is essential for practical use in partitioning a mesh-type power supply network, both for testing and diagnosis. In a mesh-type network, the defect-free IDDQ current can flow in one direction or the other depending on manufacturing variations. The current sensor must be capable of measurement over the range of IDDQ values and directions for testing purposes. For defect diagnosis, the directional capability enables the localization of the defect within the supply partition.

3. Describe the development status (i.e., concept, laboratory tested, prototype). Indicate any further development, which may be necessary.

This invention has been devised and evaluated by extensive circuit simulation. In November 1999 a design using the preferred embodiment was completed and submitted for semiconductor fabrication to the MOSIS fabrication service, using the AMI 1.5 um fabrication technology. Fabrication is expected to be complete by January 2000. The fabricated sensor will be evaluated in our laboratory to ensure that its behavior matches our simulation models. The fabricated circuit also includes the means to test some of the individual components of the invention, further validating our models. Further implementations of the invention will then be designed and fabricated using more advanced semiconductor technologies to demonstrate that the invention “scales” with technology.
4. Describe the closest known methods of performing the function of the invention and any disadvantages. Explain how the new features of the invention differ from the closest known methods. Indicate any known patents or publications, which describe such methods.

There are a large number of approaches to IDDQ current measurement that have been patented and published. These range from conventional off-chip IDDQ measurement [Maxwell 96][Wallquist 95] to on-chip measurement using built-in current sensor (BICS) circuits [Ruis 95]. Almost all of these use direct measurement by inserting the measurement tool between VCC and VSS. This measurement tool causes a voltage drop across itself, which is the input to the detection circuitry. During normal IC operation with high current transitions, this will incur a higher voltage drop across the measurement tool. This inevitably causes performance degradation, long measurement time and noise margin reduction. For BICS the performance degradation is 10-30% [Ruis 95], which is unacceptable. To reduce these effects, some approaches have incorporated a bypass element, such as a switch, capacitor, or bonding pad [Singh 95]. By this way, the perturbation in the virtual ground (or virtual supply) can be maintained below a certain level. However, as the power supply scales down, even such a voltage drop will result in severe effects on normal IC operation. Further, these bypass approaches either limit measurement speed, as in off-chip sensors, or result in large circuit area or limited placement options, as in BICSs.

There are three known approaches to measuring the IDDQ current that do not result in performance degradation. One approach is to measure the voltage drop across supply network wiring caused by the IDDQ [van Lammeren 97]. This method has been demonstrated successfully in analog circuits, but cannot be applied to digital circuits due to the much higher dynamic range of their supply currents. Two approaches have been demonstrated for measuring the IDDQ current by sensing the magnetic field using Hall magnetic field sensors [Needham 96][Nose99]. The approach of [Nose 99] is impractical since it has very low sensitivity, which results in very small output signals for IDDQ current values of interest. Our invention has more than 100 times higher sensitivity. The approach of [Needham 96] is impractical since it requires a large bias current to achieve adequate sensitivity. For typical semiconductor technologies, a bias current of 100 mA is required to achieve a 1 uV signal into the amplifier [Needham 97]. Such a current level results in an unacceptably large voltage drop across and power dissipation within the Hall sensor.

None of these inventions has ADC capability. This means that they can either provide a simple pass/fail signal when compared to a single reference value, or the sensors must be read one
at a time. Simple pass/fail signals are well known to be insufficient to adequately screen for
defective integrated circuits [Nigh 97]. Reading sensors one at a time would result in impractically
long test times for the large numbers of sensors required to achieve adequate test resolution. The
inventions also do not have full self-calibration capability, which either greatly limits their
resolution or requires that each sensor be individually calibrated, which is either impractical or
impossible. Needham’s sensor includes a reference current, but it is used to set the pass/fail limit,
not for calibration.

Popovic et al [Popovic 87] patented a magnetic field sensor using cross-coupled MAGFETs
with a feedback and amplification system. However the idea of cross-coupled MAGFETs was
already well known by that time.

Stochastic sensors are a general method of performing ADC on sensor outputs [Lin 92].
The idea of using stochastic sensors in combination with MAGFETs was described by [Hentschke
96] and other publications, for building magnetic disk drive sensing heads, but these approaches
assumed a much larger magnetic field than in our IDDQ application, and so use a much simpler
approach than our invention. In addition, these approaches assumed that the average signal value
would be zero by definition (due to the disk drive data encoding), so they could use a very simple
self-calibration scheme. These approaches were analyzed and found to be insufficient for our
application.
5. Give a complete detailed description of the best mode for practicing your invention with an emphasis on the new features or improvements over the known methods. Provide data or other evidence of the feasibility or operability of the invention. Attach any visual material that may be available such as sketches, graphs, drawings or photographs.

This invention consists of following separate components: MAFGET sensors, stochastic sensor with calibration tool, data detector, and counter/scan register. Each separate component is connected with each other as shown in Fig. 1. The MAGFET sensor detects the small IDDQ and generates a differential voltage that is coupled to stochastic sensor. The stochastic sensor consists of two flip-flop stages and a calibration tool. The stochastic sensor is used for comparing the differential MAGFET sensor signal against random Gaussian (Normal) noise on each clock cycle, and generating a random stream of bits. The probability that a bit is “0” or “1” is a function of the input signal value. If we assume that a “1” output corresponds to the MAGFET signal being greater than the noise, and associated with a positive IDDQ value, then the higher the IDDQ value, the greater the fraction of the stochastic sensor output will be a “1”. Two flip-flop stages are used to minimize the probability that the flip-flop is in a metastable state, permitting faster clock rates. The calibration tool of the stochastic sensor contributes to higher resolution of MAGFET by minimizing the inherent offset from the MAGFET sensor and stochastic sensor. The counter(scan register circuit counts the number of “1”s from the stochastic sensor. A counter value greater than N/2 for N clock cycles corresponds to a positive IDDQ value. A value less than N/2 corresponds to a negative IDDQ value. The counter value can be shifted out using scan chain circuitry. The data detector detects the high or low state of the stochastic sensor output, and increases the counter only when the stochastic sensor output transitions to a “1”. If the stochastic sensor is in a metastable state at the end of the clock cycle, the counter value remains unchanged.

The operation of a MAGFET is based on the Lorentz force on moving charge carriers (e.g. electrons or holes) caused by the magnetic field generated by an electric current. In the presence of this force, the carriers under the MOSFET channel are forced to deviate from their normal direction, resulting in a current difference at the two drains. As shown in Fig.2, the Lorentz force will be perpendicular to both the magnetic field and the direction of the carrier. A simple MAGFET structure is shown in Fig.3. The gap between the separate drains behaves as a parasitic field transistor of high channel resistance between the two adjacent drain nodes. Current crowding caused by the Lorentz force creates a current difference $\Delta I$ between the two drains. The current
difference $\Delta I$ will follow the formula $\Delta I/I \propto \mu B$, where $\mu$ is the carrier mobility and $B$ is the magnetic field strength. That is, the stronger the magnetic field, the larger the current difference.

In this invention, the MAGFETs are organized in a cross-coupled fashion as shown in Fig. 4. The PMOS and NMOS MAGFETs are shown as pairs of devices. The bias voltage generated by the inverter with input and output connected keeps both the PMOS and NMOS MAGFETs operating in the saturation region. This results in high output impedance ($R_{ch}$). Each part of the cross-coupled MAGFET is very similar in structure to CMOS inverter, which shows the current characteristic curves shown in Fig.5. When both devices are in saturation, a small current deviation of the PMOS or NMOS device gives rise to a large voltage difference due to the high output impedance ($R_{ch}$). The output voltage difference is $\Delta V = R_{ch} \cdot \Delta I$. The overall gain is dependent on the transistor parameters. In this invention we use a long gate length and wide channel MAGFETs, sizes so that the NMOS and PMOS devices have the same transconductance, which results in a gain in range of 100 dB – 120 dB, and a differential output voltage centered at $V_{CC}/2$. To maintain the cross-coupled MAGFET in high gain region, the bias transistors are the same size as the MAGFETs to bias the MAGFET gates at $V_{CC}/2$, and to track variations in the MAGFET parameters. The common mode range (CMR) of the cross-coupled MAGFETs is in range of 10-20 mV around the $V_{CC}/2$ operating point. This is sufficient to accommodate a wide range of IDDQ values.

To be a useful IDDQ measurement tool, the MAGFET sensor must have high gain and low noise. We use two approaches to increase the sensor gain, and two approaches to reduce the noise level. One method to increase gain that we have described is the cross-coupled configuration biased in the high impedance region. This doubles the gain compared to a single MAGFET. The second approach we use to increase gain is to increase the strength of the magnetic field applied to the MAGFETs, as shown in Fig. 4-1. The magnetic field strength is inversely proportional to the distance away from the current source. To maximize the magnetic field strength at the MAGFETs, the layer carrying IDDQ is just above the MAGFET gate. In addition, the Lorentz force is proportional to the carrier velocity. Since this velocity is highest in the transistor channel near the drain, the MAGFETs are oriented so that their drains are adjacent to the IDDQ source. Thus the highest velocity carriers see the strongest magnetic field, maximizing the Lorentz force and thus the current difference. A further enhancement is to locate the drain contacts near the drain air gap,
resulting in current crowding in this region. As a result, the carriers must be deflected a smaller
distance to one drain or the other, maximizing the current difference for a given magnetic field.

The IDDQ range of interest generates a very small magnetic field. This field is much
smaller than the Earth’s magnetic field, $B_{\text{earth}}$, or fields generated by nearby electrical equipment.
To cancel out these external magnetic fields, a second pair of cross-coupled MAGFETs is located
on the opposite side of the IDDQ source, and the outputs connected to the other MAGFET pair
outputs in reverse order, as shown in Fig. 4-1. Since the field generated by the IDDQ is in the
opposite direction on each MAGFET pair, their differential signals have the same value. But an
external common-mode field results in opposite differential signals, so the external field does not
result in a net MAGFET sensor signal [Needham 96].

A second major noise source is the intrinsic noise of the MOSFET circuitry. The two major
noise components of a MOSFET are classified as $1/f$ (or flicker) noise and thermal noise. It is well
known that $1/f$ noise is dominant at low frequencies and thermal noise at high frequencies. The $1/f$
noise amplitude falls rapidly with frequency and is negligible after several kHz. Thermal noise is
Normally distributed with constant noise amplitude across the frequency range. The operating
frequency of the MAGFETs in this invention will be no more than a few kHz, as determined by the
IDDQ test speed. Due to their high output impedance and low frequency operation, the MAGFET
$1/f$ noise dominates the IDDQ sensor noise. To minimize this noise, this invention places a load
capacitor ($C_{\text{load}}$) between the MAGFET (Fig. 4) and the stochastic sensor. In combination with the
MAGFET output impedance ($R_{\text{ch}}$), this creates a low pass filter (LPF) to attenuate noise above the
MAGFET operating frequency range. Since $R_{\text{ch}}$ is large, $C_{\text{load}}$ is relatively small.

Despite the above design efforts, the SNR from the MAGFET sensor is much lower than 1,
and too small to be practically amplified by traditional analog methods. In this invention, a
stochastic sensor in combination with a counter is used to convert the MAGFET sensor differential
analog signal to a digital value. The stochastic sensor achieves high sensitivity and high noise
immunity through repetition. It repeatedly performs a comparison of a measured signal and a
random signal (noise in this case). Since the noise has a Normal PDF (Probability Density
Function), the sensor produces a random bit stream with a Normal PDF. It represents an equivalent
picture of the analog input signal. For a given SNR (signal to noise), the number of clock cycles
(repetitions), $N$, to be done is defined as follows:

$$N = \frac{C}{(\text{SNR})^2}$$
In this equation $C$ is a constant that depends on the desired confidence interval of the result [Lin 92]. For the resolution requirements of IDDQ testing, $C$ is about 64. For an SNR of 0.01, about 640,000 clock cycles are required to achieve the desired resolution. The output of the MAGFET sensor is directly coupled to the stochastic sensor. The stochastic sensor performs the comparison of both input signals at every clock and sends the results as either VCC (“1”) or VSS (“0”). In the operation of the stochastic sensor, the sensing time is very important because it will determine the clock cycle time and thus the IDDQ test speed. If the sensing time is too long for a given clock cycle time, the sensor will have a high probability of remaining in the metastable state. This is equivalent to a “don’t know” output rather than a “1” or “0”, and introduces an error in the ADC process. This invention minimizes the sensing time by adopting a two-stage stochastic sensor, with each stage operating in opposite phase (Fig.1). The first stage is active during clock "high” and disabled during clockb "high”. The second stage will take the outputs of the first stage as inputs and be active during clockb "high”. During clockb "high", the return of the first stage to the pre-charge state will not affect the second stage because the output of the first flip-flop sensor is connected to the gate input of the second stage. Using this two-stage approach, the available sensing time of the stochastic sensor becomes twice that of a single-stage sensor. The output of the second stage is connected to the counter/scan register, which counts the number of “1” values determined by the comparison between the MAGFET sensor signal and noise. The counter result represents the relative magnitude of the IDDQ current compared to reference current $I_{ref}$. That is, the condition that the counter value is greater than half the number of cycles means that the IDDQ current is greater than $I_{ref}$. A scan chain is used to send the counter value outside the chip. This invention combines the counter and scan register into one (Fig.6 counter/scan register) to reduce the area. During the scanning mode, the counter will act like a scan-in register and be reset to zero. During the normal operation of the stochastic sensor, the counter acts as a counter, and in successive scan out mode, outputs the counter results serially as a scan register.

The stochastic sensor of this invention must be very precise because it compares very small signals and any error will directly show up as an error in the IDDQ measurement. But there are mismatches in the stochastic sensor and MAGFET sensor circuitry caused by process variation and mismatches from layout design. Thus the sensor must be calibrated. To get a precise calibration tool, on-chip self-calibration has advantages over external calibration. On-chip calibration can be done in parallel for all IDDQ sensors, and avoids the noise pickup associated with external signals.
The self-calibration of this invention is automatically done in the first stage of the stochastic sensor using the charge pumping method. The first stage consists of a pure stochastic sensor part and a charge-controlled calibration transistor part (pull down NMOSFET in Fig. 9). Assuming that the calibration transistor operates in the ohmic region, gate-source voltage variation is converted into drain-source voltage variation. The drain-source voltage variation is used to fix the sensor mismatch by changing the gate-source voltage of the NMOSFETs of the sensor part. The gate-source voltage of the calibration transistors is varied very precisely by charge pumping method. The smallest calibration voltage level is determined by the ratio of the charge on the reservoir capacitor to the pumping charge per cycle. The bias stages, reservoir capacitor and charge up/down transistor are well balanced to both VCC and VSS so that during a normal (non-calibration) clock cycle, charge leakage from VCC to VSS are well balanced through circuit design and layout techniques. The reservoir capacitor size is also large enough that the leakage is small relative to this capacity. This is increasingly important with thinner gate oxides, and is necessary for the stochastic sensor to remain in calibration long enough to complete many IDDQ tests. The calibration sequence is as follows:

1. The IDDQ current is shut off. If the IDDQ sensor is built-in, this requires a separate power supply partition for the logic under test.
2. The bias stage is controlled by a power-up signal, which detects the stability of the power supply on chip.
3. During the power-up sequence, the path from VCC through the bias node to ground is on and decides it's final voltage.
4. After power-up, the calibration will be done using the calibration enable signal.
5. Calibration will be terminated externally by the calibration disable signal.

Fig. 8 shows the timing diagram of the IDDQ test scheme proposed in this invention. The power-up signal will be generated internally or externally and used to initially charge the bias nodes of the calibration tool. Right after power-up, CLK and CLKB will be applied to enable the sense amplifier during calibration mode or normal operation mode. CALB controls the start and the end of calibration. During CALB enable (“1”), the stochastic sensor performs calibration. Upon the end of calibration, scan-in mode will be entered by SCAN/SCANB to reset the counter to “0”. SCANIN-PAD will be used to input the data stream to counter serially. During scan mode, the clock signals Q1/Q1B and Q2/Q2B are used to control the scan register. In this mode, the counter
will act like a scan register shifting data at every Q clock. At the same time, the counter result is scanned out serially. Now, the condition for sensing and measuring the IDDQ current is completely set up. During sensing mode, the counter mode of counter/scan register will be on and act as a counter accumulating results from the stochastic sensor.
6. State the advantages of your invention over what has been done before, the problems it solves, or new applications achieved. Indicate any disadvantages or limitations and explain how they might be overcome.

As described above, this invention measures IDDQ current by using the magnetic field. It is a noninvasive method that does not disturb signal sources. The prior art by Needham et al [Needham 96] uses a Hall sensor to measure IDDQ using Hall effect. It uses a silicon Hall sensor, which induces a voltage difference at the two ends of the whole sensor by the current passing through it. In Needham's invention, the sensor outputs are coupled to an amplifier, which amplifies the signal difference. However, Needham's invention does not have any means to improve resolution. The Hall sensor itself has relatively low resolution for practical bias current levels. The Hall sensor will be exposed to numerous noise sources and have inherited noise sources such as flicker noise, thermal noise etc. Furthermore, it does not have any means to compensate for the offset of amplifier or Hall sensor. Inevitably, it will show poor resolution of IDDQ measurement. The prior art by Nose and Sakurai [Nose 99] uses Hall sensors built using transistor channels, without any amplification. While very small, these have very low resolution.

Our invention adopts a stochastic sensor as a post-processor to MAGFET sensor. This invention has an extra capacitor between the MAGFET sensor and stochastic sensor creating a low pass filter to block noise above the frequency range of interest. This reduces the amount of noise introduced into the stochastic sensor. Based on this, our invention can measure a signal level that is much smaller than noise. This invention is expected to measure signals as small as 1/200 of the signal-to-noise ration (SNR). The stochastic sensor is equipped with an offset calibration tool to compensate for the offset from process variation or layout mismatch. In order to achieve a resolution of 1/200 of the SNR, simulations indicate that a counter(scan register as long as 20 bits is needed. The actual length depends on the noise level in the circuit and the resolution requirements. Because the stochastic sensor decision probability follows the Normal distribution, the counter value will also be Normally distributed. This invention employs 2 successive stochastic sensors to compare the IDDQ level with $I_{ref}$ and the circuit noise. Two successive sensors will reduce the time that the stochastic sensor spends in the metastable state, permitting higher clock rates and shorter measurement times.

This invention also has a capability to diagnose the defected chip. This is achieved both by scanning out all scan registers to identify which power supply partitions have faulty current values,
and by measuring the current direct to identify the overall direction of current flow within a mesh network.

7. Indicate any alternate embodiments, procedures or methods of construction for the invention.

The invention is described in section 5 using CMOS technology. Alternate implementations can be developed using complementary GaAs. The higher mobility of the GaAs MESFET transistor will result in even higher signal gain in the MAGFET sensor than a CMOS implementation.

There are several different possible layout configurations of the MAGFET sensor to cancel outside noise effects. All that is required is that the outside noise be seen as common mode to each of the differential signals, so that it cancels out.

Alternative MAGFET orientations configure their current flow to be in parallel with the IDDQ current, or perpendicular with the current flowing away from the supply line (the MAGFET source is closest to the supply line). These configurations will result in lower gain, but may be desirable for layout area reasons.

The MAGFET sensor can be implemented with the output connected to the MAGFET gate inputs, rather than using a bias voltage. This feedback path can potentially achieve higher gain, but potentially makes it more difficult to shut off the MAGFET sensor bias current when the IDDQ sensor is inactive.

There are several different circuit configurations that can implement the stochastic sensor. The second stage of the sensor can be omitted for a smaller circuit size, but lower speed of operation.

There are several different circuit configurations that can implement the self-calibration tool. Rather than placing the calibration transistors in series with the pulldown paths of the stochastic sensor, the transistors can be placed in parallel. If a floating-gate MOSFET technology is available, such as a flash process, the calibration tool can be implemented to program the gate voltage of the stochastic sensor calibration transistors. The advantage of this approach is that calibration need only be done once, rather than just prior to a series of measurements. The disadvantage is the larger circuit area to implement the high-voltage programming signals.
The counter/scan register can be modified to have a parallel load function added. This permits the counter/scan register to be shared by the chip logic if the IDDQ sensor is used as a built-in current sensor. During normal chip operation, the counter/scan register is used as a normal scan register. Whenever an IDDQ test is to be performed, the logic values are scanned out and saved, and at the same time “0”s are scanned in to reset the counter. IDDQ testing is performed, and then the counter value is scanned out, and at the same time the saved logic values are scanned back in. Since the scan/counter register can dominate the IDDQ sensor size, being able to share it with normal chip logic greatly reduces the chip area overhead for IDDQ testing. The only restriction is that the scan/counter register must be located close enough to the stochastic sensor that the wire length does not reduce the stochastic sensor clock rate.

8. Identify the grants, contracts, or other sources of funding contributing to the conception and development of the invention. Indicate if the invention was made as part of one's assigned duties or with the use of Texas A&M University System facilities or services.

This invention was developed using funding from the National Science Foundation under projects 32525-45820 and 32525-59180. The invention was developed as part of the inventors’ duties as TEES employees, using TEES facilities.

9. If work on the invention is to be continued, indicate the sources of funding and the nature of the work.

Further research is being performed on alternate embodiments, and optimizing the preferred embodiment for different semiconductor technologies. Research is also being performed on the usage methodology in terms of setting pass/fail testing limits and automatic insertion of the invention into IC power supply networks. This research is funded by the National Science Foundation under project 32525-59180.

10. Provide name and date of any publications or abstracts (oral or written) as well as any proposed publications which mention or describe the invention. Separate general publications from those, which disclose the critical elements of the invention.

National Science Foundation proposals 9870757, submitted 12/19/97, and proposal 9971192, submitted 10/27/99, disclosed the critical elements of the invention in its early conceptual
form (which is not the current preferred embodiment). The program manager (Robert Grafton), administrative personnel, and referees who viewed the documents signed standard NSF confidentiality agreements regarding proposal content. Semiconductor Research Corporation white papers, dated 5/7/98 and 6/18/98, briefly disclosed the critical elements in prototype form with a small schematic and few paragraphs. SRC program managers (Justin Harlow and William Joyner) viewed these documents under the standard SRC proposal confidentiality guidelines. The white papers referenced a TEES Web site that provided a list of references to prior art.

Wayne Needham of Intel first described the idea of an IDDQ sensor using magnetic fields to Dr. Walker at the 1997 VLSI Test Symposium (April 28-May 1, 1997). A second meeting was held on 5/28/97 in Austin at the US Workshop of the 1997 National Technology Roadmap for Semiconductor. At that time Mr. Needham described his prior art, and provided some additional documentation describing his calculations [Needham 97]. His experimental results were not promising, he had lost internal support (at Intel) to continue the research, and suggested that Dr. Walker work on the problem. Mr. Needham offered to provide Dr. Walker with his experimental results, but Mr. Needham retired from Intel before that could be done. Dr. Walker and Mr. Needham exchanged some e-mail during May and June 1997 to clarify Mr. Needham’s patent.

One of Dr. Walker’s graduate students, Shashidhar Rajamani, was assigned the problem of working on an IDDQ sensor using magnetic fields. He identified prior art on sensing magnetic fields using stochastic sensors, but made no progress in terms of research, and left Texas A&M without completing a degree.

The fact that we were working on IDDQ sensors using magnetic fields was disclosed orally by Dr. Walker to colleagues at the VTS98, VTS99, ITC98 and ITC99 conferences, and in transparencies during a talk at the Die Products Consortium meeting on 11/3/99. No details beyond this were given. An email message of 12/19/97 disclosed the fact that we were working on IDDQ sensors to Don Ross of Mentor Graphics. Again, no details were provided.

A test chip containing an implementation of the invention was submitted for fabrication to the MOSIS service on 11/15/99. This disclosure took the form of a mask work. The MOSIS customer agreement requires them to keep all design data confidential, and for them to reach such agreements with their suppliers.
In summary, the details of the invention were only disclosed in the NSF and SRC proposals cited above, and the mask work submitted to MOSIS. In all cases, confidentiality agreements forbid disclosure to others.

11. Chronology of principal events in conception and development:

(a) Earliest conception date. Is there substantiating evidence such as a notebook or a witness?

The earliest conception date of the full embodiment was in Fall 1997. This is documented by working notes, and the NSF proposal dated 12/19/97.

(b) Dates of oral or written disclosures to other persons and names of such persons.

The only disclosures of the invention were those of its early concept in the proposals and the test chip mask work cited above.

(c) First written record and availability of such records.

The earliest record of the start of this research is an email message dated 5/2/97. The first written record of a complete embodiment is the NSF proposal dated 12/19/97.

(d) Dates and results of first test of invention and first successful test.

A test chip was submitted to MOSIS on 11/15/99, and should be received back for testing in January 2000. Extensive simulations and analysis were carried out of the preferred embodiment during late 1998 and Spring and Fall 1999. (Mr. Kim was an employee of IBM during Summer 1999 working on another unrelated project).

12. Joint inventors should briefly describe each of their contributions to the conception of the invention and the percentage of effort for each (totaling 100%).

The invention was 50% developed by Dr. Walker (background, need, initial embodiment concepts), and 50% by Mr. Kim (detailed analysis of embodiment alternatives and development of final invention details and preferred embodiment).
References


Each inventor should sign and date the last page of the disclosure. Additionally, the invention disclosure should then be read and signed by a witness who understands it, using the following statement:

____________________________________    ____________
Duncan M. Walker                                              12/8/1999

____________________________________    ____________
Hoki Kim                                                             12/8/1999

Disclosed to and understood by me this _______ day of ____________, ______.
Signature: ________________________(WITNESS)_____________________________
Fig. 1 Proposed IDDQ Sensor

Fig. 2 Lorentz Force on moving charge
Fig. 3 Simple MAGFET structure

Fig. 4 Cross-Coupled MAGFET Sensor
Fig. 4-1 Cross-Coupled MAGFET Sensor

Fig. 5 Current characteristic of CMOS Inverter
Fig. 6 Unit stage of counter & scan register

Fig. 7 Counter & scan register
Fig. 8 Timing Diagram

Fig. 9 1sT Stochastic Sensor (with calibration tool)
Fig. 10 Data Detector